Final Technical Report

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U.S. DEPARTMENT OF ENERGY

Sandia National Laboratories

Executive Summary:

Increasing the penetration of distributed renewable sources, including photovoltaic (PV) generators, poses technical challenges for grid management. The grid has been optimized over decades to rely on large centralized power plants with well-established feedback controls. Conventional generators provide relatively constant dispatchable power and help to regulate both voltage and frequency. In contrast, photovoltaic (PV) power is variable, is only as predictable as the weather, and provides no control action. Thus, as conventional generation is displaced by PV power, utility operation stake holders are concerned about managing fluctuations in grid voltage and frequency. Furthermore, since the operation of these distributed resources are bound by certain rules that require they stop delivering power when measured voltage or frequency deviate from the nominal operating point, there are also concerns that a single grid event may cause a large fraction of generation to turn off, triggering a black out or break-up of an electric power system.

To mitigate effects on grid voltage and frequency due to increased penetration of distributed energy resources (DERs), new grid support functions (GSFs) have been investigated to allow DERs to participate in voltage and frequency regulation. In addition, new voltage and frequency ride-through (V/FRT) functions are being developed to enable these inverters to remain connected even when voltage and frequency deviate considerably. Unfortunately, the implementation of these functions brings with it a new set of engineering concerns including an increased propensity to unintentionally island, the need to ensure standards of performance, as well as interoperability of multiple inverters on one bus, dynamic response of inverters to load rejection and ground fault, and finally how to address the cyber security threat. To accelerate advanced inverter adoption, this project addresses these potential obstacles, thus enabling increased PV penetration.

This project was successful in developing both general/generic and manufacturer-specific transient inverter models and adapting them to include GSFs and V/FRT capability to aid in extensive simulation studies of anti-islanding efficacy. Simulation and experimental studies were done to investigate efficacy of existing anti-islanding schemes and quantify performance. In addition, two new anti-islanding methods were developed and tested in the lab that are robust against the effects of GSFs and V/FRT and are expected to be cost-effective. Furthermore, an extensive testing protocol was developed in collaboration with industry, documented, and applied to commercial and pre-commercial inverters. This test protocol is a potential means by which to certify grid-connected equipment for GSF and V/FRT implementation and ensure a prescribed standard of performance. Finally, a Sandia team began the evaluation of cybersecurity implications of remote commands to DERs implementing GSFs and V/FRT functions.

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Background:

As more distributed renewable generation is incorporated into the grid, well-regulated conventional generation will be displaced by stochastic energy sources, which are likely to contribute to voltage and frequency regulation difficulties [1]-[3]. Negative impacts of high penetration PV may also include reverse power flow, power fluctuations, power factor changes, unintentional islanding, and fault currents [4]. In addition recent studies that consider the impact of PV on low frequency inter-area modes have even reported that greater PV penetration may "detrimentally effect the inter-area mode" through reduction in damping [4]. In [5], the authors list four mechanisms by which PV and similar converter systems may affect system damping; therein, the authors discover the potential for new oscillatory modes.

Grid Support Functions and Ride-Through

Anticipating the high penetration of PV DER has thus led to significant changes in utility interconnection requirements that include voltage and frequency regulation requirements and robustness to voltage and frequency disturbance. These changes require new advanced inverter functions which include grid support functions that help regulate voltage and frequency as well as voltage and frequency ride through requirements. One approach for PV DER to provide grid support is to modulate active and reactive power based on the volt-var and frequency-watt characteristics shown in Figure 1 [6],[7]. In these functions, one notes a deadband region around the nominal frequency and voltage; outside this region, negative feedback is applied to mitigate deviations, up to converter limits. These functions, in part, replace the control efforts lost by displacing conventional generation.

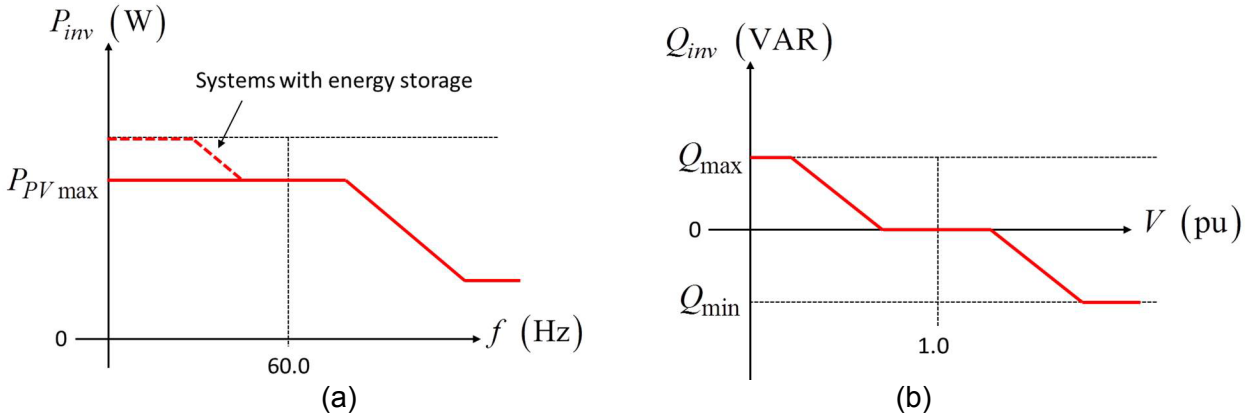
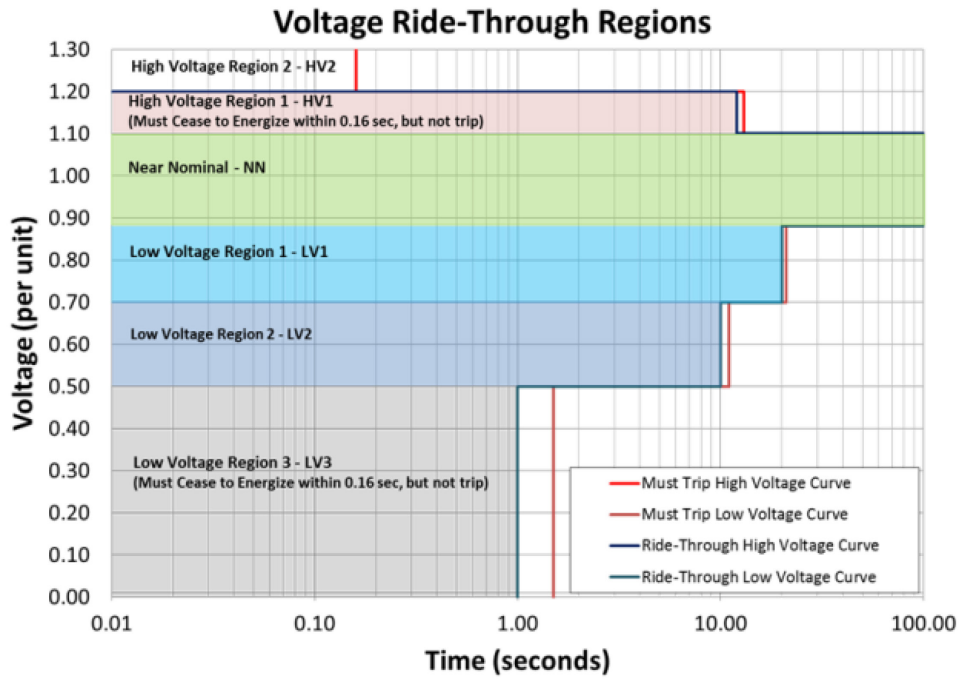
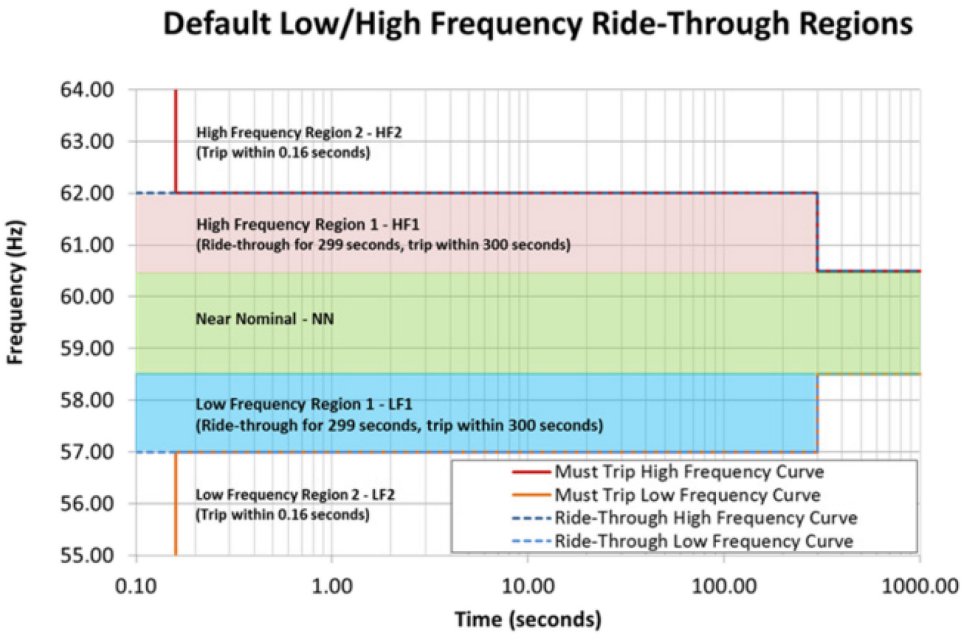


Figure 1. Illustration of Grid support functions: (a) frequency-watt and (b) volt-var

Frequency and voltage ride through allows inverters to remain connected to ensure robust recovery in the event of voltage and frequency disturbances; see Figure 2 [6]. Therein, it is noted that the severity and duration of frequency and voltage deviations are considered together. Long and/or severe deviations result in disconnection of the resource. The implementation of ride-through requires the DER to tolerate larger and longer deviations to prevent large scale outages from being triggered by a minor grid event.



(a)



(b)

Figure 2. Illustration of voltage and frequency ride-through (V/FRT) characteristics for (a) Voltage and (b) Frequency

Implementing these advanced capabilities is essential to mitigating the negative impacts of high penetration PV, but their integration into a practical system presents

technical challenges. One concern is evaluating whether manufacturers can even implement the functions in a manner that meets specifications. The second concern is the increased risk of unintentional islanding due to the stabilizing effects of grid support functions and the increased disturbance tolerance afforded by ride-through capability. The efforts of this project are divided into three tasks. Tasks 1 and 2 address the islanding issue in two parallel efforts while Task 3 is concerned with standards development and demonstration of advanced functions on manufacturer hardware.

Island detection schemes are designed to detect an islanding condition in grid connected systems so that such systems can shut down when the utility connection is broken, in order to prevent potential damage to equipment and infrastructure and risk to personnel caused when the utility power is later reconnected.

Anti-Islanding Using Communication methods

Task 1 of this project concerned two island detection methods that rely on communications between distribution/transmission components and the inverter to establish whether an island has occurred: Power Line Carrier (PLC) and Synchro Phasor (SP). In general, it was found that most researchers pursuing the use of PLC technology to do island detection have been focusing on high frequency carrier signals [8]-[10], resulting in efforts being spent on solving problems associated with high-frequency propagation [8], interference [9] or on sophisticated implementations to bypass transformers using wireless [10]. Specifically, in [9], laboratory measurements taken of conducted emissions from compact fluorescent bulbs (CLF) indicate the potential for these devices to interfere with powerline communications in the CENELEC band: 150 kHz-30 Mhz is high and thus erodes the signal to noise ratio. The potential for interference from so many active power electronic converters in proximity to distributed generation reinforces the motivation to select a low-frequency permissive signal. In addition, research on high frequency characteristics of cable (not specific to PLC) predict large attenuation levels in high frequency signals as well. In [12], an in depth analysis is done of shielded medium voltage (MV) power cable to determine its high frequency characteristics. In particular, the composite “loss budget”, indicates a 2 dB/km attenuation at 150 kHz in new cable, while related publications on trending dielectric loss [13] suggest at least a ten-fold increase in losses after 10 years of service aging of a typical XLPE cable due to water tree degradation, which would amount to a 22 dB/km loss at 150 kHz. In contrast, the attenuation of sub-harmonics (or undertones), if estimated using the value at 100 Hz, is approximately 0.1 dB/km. This suggests that a subharmonic permissive signal will propagate much further, resulting in fewer transmitters needing to be installed. These results reinforce the current effort to investigate methods based on sub-harmonic carrier permissive signals since the lower frequency signal travels further and can pass through distribution-level transformers. In addition, since the method involves series voltage injection, the magnetic components of the system will be significantly smaller than those used in current injection based approaches such as the method based on that used for automatic meter reading [14],[15]. One concern with the PLC approach, however, is with maintaining compliance with the IEEE 1453-2004 flicker standard [16]. For a 17 Hz voltage injection, which is

the target frequency used herein, the tolerance is 0.737% and 0.530% of voltage at 120V and 230V respectively [15]. This will limit the 17 Hz voltage to a maximum value of 0.884V or 1.22V at the respective voltages. The SNR consideration is the obvious: there must be enough 17 Hz signal present that it is detectable at all endpoints. This consideration would suggest that the largest possible value of 17 Hz signal be used, but the maximum is constrained by flicker considerations.

The use of SynchroPhasor measurements to detect an islanding condition is a fairly new idea [17]-[20]. When two electrical areas are connected in an AC network, the frequency and angle differences are bounded. The SynchroPhasor (SP) based island detection methods rely upon data from two different phasor measurement units (PMUs) to detect whether the two electrical regions are connected; see Figure 3. Unfortunately, SP methods have classically relied on GPS time synchronization. This issue does not impact the systems likelihood to detect an island; rather, if signals are not synchronized, an event on the grid may cause a false-trigger since the time shift results in large frequency and angle areas.

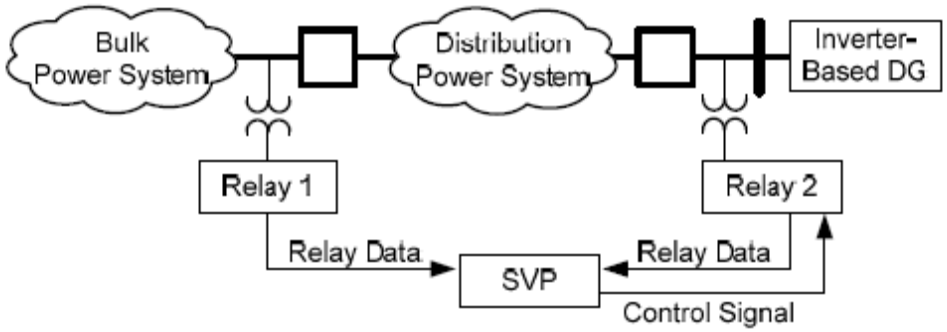


Figure 3. Illustration of SP island detection method showing PMUs located in two areas [19]

In [17], the SynchroPhasor-based anti-islanding approach is discussed and contrasted with passive and active anti-islanding methods as well as PLC. Therein, the authors implement three algorithms: (1) absolute phase angle difference (APAD), (2) wide area method (WAM) where PMU differences are plotted in the slip-acceleration plane, and correlation coefficient based method (CCB) where relative frequencies are correlated. APAD and WAM are both fast-acting; though APAD may be overly-sensitive to grid disturbances. CCB is sometimes slower than the other two methods and doesn't have a predetermined run-time. The authors of [18] describe a SynchroPhasor based island detection scheme that uses both absolute angle differences and defines a pair of decision boundaries, termed "Islanding Zone A" and "Islanding Zone B" in the slip-acceleration phase plane (a variation of what's presented in [17]). The benefit of this approach is that it is potentially more robust against transients that effect synchronous generators, and it tends to detect an island within 400 msec (including 100 msec network delays), and over 10 times faster than absolute phase angle difference alone. The disadvantage with this technique as with all techniques reported in [17]-[20] is the heavy reliance on GPS time synchronization.

In this project, efforts are focused on the evaluation of SynchroPhasor methods for their robustness to GPS time-slip and potential solutions are posed that do not require GPS synchronization. In particular, the slip-acceleration method, the CCB method, and a new method termed Integrated Frequency Error (IFE), developed by NPPT, are being investigated in collaboration with Sandia for their false-trip susceptibilities in the event of relative GPS time-slip in the PMU clock(s).

Anti-Islanding Using Autonomous methods

The vast majority of island detection schemes use so-called “autonomous” methods. In particular, interconnection standards require such systems to stop supplying power, within a certain duration, when the grid is disconnected [21], and a test has been developed for establishing compliance [22]-[24]. Several methods exist to prevent an islanding condition, including passive and active methods [22]-[26]. Each method operates by sensing and differentiating inverter dynamics when grid-connected versus islanding condition. However, since new advanced inverter functions are intended to emulate generator controls, a grid disconnection may be more difficult to detect with these in operation. The inverter would be simultaneously trying to mitigate disturbances and creating disturbances to test the stiffness of grid connection. This contradiction has put some manufacturers at an impasse. Thus, this project is developing collaborative autonomous controls that allow the island detection and the grid support functions to operate together. Other concerns have also been cited such as the potential for positive feedback schemes to destabilize distributed generation. For example, in [27], the authors study positive feedback anti-islanding methods in inverter-based distributed generation using eigenanalysis and simulation of both a small-signal model and a detailed Matlab/Simulink model. Therein, the authors conclude that “…strong positive feedback of the anti-islanding scheme will destabilize the grid-connected DG system when the grid is weak and the local load level is high.” The development of collaborative controls is intended to mitigate these issues by designing both functions into one feedback control law.

Performance Protocol Development

As standards continue to evolve, it is necessary to develop test protocols to independently verify that the inverters are properly executing the advanced functions. Interoperability is assured by establishing common definitions for the functions and a method to test compliance with operational requirements. This document describes test protocols developed by SNL to evaluate the electrical performance and operational capabilities of PV inverters and energy storage, as described in IEC TR 61850-90-7 [31]. While many of these functions are not currently required by existing grid codes or may not be widely available commercially, the industry is rapidly moving in that direction. Interoperability issues are already apparent as some of these inverter capabilities are being incorporated in large demonstration and commercial projects. The test protocols are intended to be used to verify acceptable performance of inverters within the standard framework described in IEC TR 61850-90-7. These test protocols,

as they are refined and validated over time, can become precursors for future certification test procedures for DER advanced grid support functions.

The test protocols establish a common set of procedures to verify through direct testing conformance with respect to the functions described in IEC TR 61850-90-7. Verification of compliance of a certain device or EUT involves testing two performance aspects:

(1) Communications – determining whether and how the EUT is receiving and understanding the request or input (communications);

(2) Electrical – determining if the EUT responds appropriately to the input(s) by initiating the correct commands to the electrical and mechanical equipment (control logic), and whether the equipment responds properly to those control commands.

The communications aspects of the interoperability testing will be to verify that the EUT can process inputs provided using a standard communications format. The electrical aspects will examine how the EUT performs the functions or task(s) listed in IEC TR 61850-90-7. (A test protocol for an additional function, Low/High Frequency Ride Through – L/HFRT – has also been developed, as the California Energy Commission and the California Public Utilities Commission are considering making a L/HFRT a required function for DER inverters under their Rule 21.)

Transient Overvoltage

In addition, recent concerns have been raised over the potential of DERs to cause a transient overvoltage (TrOV) condition, which could jeopardize the integrity of customer or utility equipment. TrOV has become one of the most limiting factors to achieve penetration levels beyond 100% of daytime minimum load. A TrOV may be caused by (1) a ground fault overvoltage (GFO) that can occur during single phase to ground faults or (2) a load rejection overvoltage (LRO) that can happen if an island is formed that has a high generation-to-load ratio. The TrOV problem has been studied fairly extensively for rotating machines, and codes and standards such as IEEE 142 have been developed. However, inverters are very different, and the existing body of knowledge cannot be directly applied to them. The TrOV issue is a nascent concern that has motivated many in the community to recommend expensive grounding techniques to mitigate the effect. Potentially, this concern can be addressed by standardizing the TrOV response limits.

In [28], the authors investigate GFO and LRO problems with a commercial inverter and cite several issues. Primarily, there is no existing standard for inverter TrOV; they note that the closest standard is the CBEMA curve, which was designed for electronics in the 1980's. In addition, the mitigation plan implemented by the authors included a reduction in the over-voltage trigger level, raising a concern over nuisance tripping. This, in particular, could contradict the implementation of HVRT.

In [29], the authors investigate dynamic changes in voltage following a fault for systems employing fault ride through (FRT). Studies were done through simulations of realistic models of systems that included both medium and high voltage components. Therein, it was noted that with "… high penetration of PV, the post-disturbance steady-

state load bus voltage could be higher than 110% …" In this case, the FRT scheme was effectively an LVRT, and the elevated voltage was sustained after the fault cleared. This would, using recently developed terms, be more of a *temporary overvoltage* (TOV), rather than a TrOV. It is, nonetheless, relevant when considering the total behavior of the power system during and after a fault when advanced functionality is implemented. In a recent report released by NREL in collaboration with SolarCity [30], the results of a rather comprehensive LRO study were presented. Therein, test results included five commercial units, 11 power/loading scenarios, each repeated several times. The results are consistent with initial tests done at Sandia (DETL) and reported in the Q1 report that the LRO concerns may be overstated. Therein, the worst-case result was a 200% overvoltage, but the typical values were quite a bit smaller. Thus, the concern remains, but the typical voltage amplitudes are less than anticipated.

The draft Performance Test Protocol for Evaluating Inverters Used in Grid-Connected Photovoltaic Systems has undergone revisions to address the non-unity power factor operation of inverters. The changes will introduce additional test requirements to determine the conversion efficiency of PV inverters and the document has been submitted to UL. The process to turn this draft document into a testing standard requires the document to be submitted to the standards technical panel (STP) and undergo a commenting period followed by a revision to address any issues.

Cyber Security

The integration of advanced inverters into distributed generation power systems creates new avenues for malicious attack that did not exist in past generations of inverters. Further, distributed generation solar power networks pose unique challenges to cybersecurity which arise due to a lack of physical security and a relatively large number cyber-attack targets. Unfortunately, specific research on the cyber security implications for advanced inverters is hard to come by and rarely thorough enough to report on.

The critical nature of an energy grid infrastructure creates an environment in which the smart energy grid becomes a prime target for cyber terrorism. Wide area solar networks contain assets that range from solar panels, substations, control centers, human machine interfaces, log servers, advanced inverters, etc., all of which are potential avenues of malicious attack. Distributed solar resources are particularly susceptible to both physical and cyber-attacks. This equates to a more vulnerable network in which embedded devices with bi-directional communication are at greater risk [32]. A more comprehensive background is provided in [33].

Project Objectives:

To mitigate effects on grid voltage and frequency due to increased penetration of distributed energy resources (DERs), new advanced inverter functions have been investigated to allow DERs to participate in voltage and frequency regulation. However, the implementation of advanced inverter functions creates new engineering challenges. The goal of this project is to address these engineering challenges and enable advanced inverter adoption. Specifically, this project addresses anti-islanding compliance, establishment of test protocols that help define a certification procedure for grid-connected DERs and ensure the quality of advanced inverter function operation in the grid, and development of standard communication protocols for advanced function implementation with some attention given to cyber security issues.

Anti-Islanding Technology Development Goals

All distributed PV sources must comply with anti-islanding standards (run-on-times (ROTs) <2 sec). Unfortunately, the incorporation of advanced inverter capabilities can interfere with anti-islanding schemes. These new capabilities include grid support functions (GSFs) like volt/VAr and frequency/watt as well as wider limits on allowable voltage and frequency (ie voltage and frequency ride through (V/FRT)). The goals of this project include developing a better understanding of how GSFs and V/FRT might interfere with anti-islanding, the quantification of the effect of GSFs and V/FRT on island detection, the investigation of SynchroPhasor-based island-detection, and the development of alternative anti-islanding schemes including powerline carrier (PLC) and Collaborative Controls. Each of these methods is robust against GSF and V/FRT interactions for different reasons. The anti-islanding work spans tasks 1 and 2, and the goals of these tasks are both: (1) to clarify the effect of GSFs and V/FRT on anti-islanding in single and multi-inverter implementations and (2) to develop or identify one or more anti-islanding methods that are better suited for advanced inverter implementation. This work includes extensive modeling and simulation work to assess anti-islanding performance, testing of manufacturer hardware to assess anti-islanding performance, and development of new anti-islanding hardware prototypes.

Test Protocol Development Goals

Facilitating the full functionality of distributed energy resources on the utility grid requires new EPS support functions capabilities to be fully assessed and analyzed to ensure functions meet utility interconnection requirements. The utilization of EPS support functions is enabled through a secure and reliable communication based activation of advanced inverter functions. The test protocol is designed to provide a thorough assessment of the inverters advanced capabilities, which have been developed to meet IEC 61850-90-7 requirements. A crucial part of the test procedure development includes validating the test procedure while assessing industry partners' equipment and laboratory equipment that is readily available for this purpose and assessing the testability of the test protocol. One goal of this effort is raise the technical readiness of this draft test procedure for eventual standardization. The SNL interoperability test protocol is currently utilized to assess the capabilities on pre-

production hardware but will form the basis for UL certification standards in the future. Another goal is the development of a communication protocol; this will guide how US utilities deploy advanced inverter functions through interoperability communication links.

This effort comprises task 3. This includes extensive experimentation using manufacturer commercial and pre-commercial hardware, and participation in industry forums and IEEE working groups.

The project tasks and milestones are given as follows:

1. Task 1 – Anti-Islanding Technology Development
    1. Inverter Model Development
    2. Multi-Inverter anti-islanding performance assessment
    3. Lab Demonstration of Power Line Carrier (PLC) based island detection
    4. Evaluate SynchroPhasor anti-islanding efficacy with GPS timeslip

    Milestone 1– Report on anti-islanding performance
    Milestones 2-3 – Demonstrate and quantify PLC performance
    Milestone 4 - Establish utility benefit to PLC method
2. Task 2 – Autonomous Inverter Controls Based Anti-Islanding Technology
    1. Development of volt/VAr, V/FRT detailed models
    2. Development of Collaborative Anti-Islanding controls

    Milestone 1 – Coordinated Controls Tech advance
    Milestone 2 – Demonstrate Coordinated Controls with commercial system(s) in simulation
    Milestone 3 – Demonstrate Collaborative Controls in hardware
    Milestone 4 – Submit provisional patent for collaborative controls
3. Task 3 - Grid Interoperability test protocol development for advanced functions
    1. Test protocol development
    2. Lead implementation of test protocol into new standards
    3. Investigate/Develop Transient overvoltage mitigation strategies

    Milestone 1- Report on Advanced Inverter implementation
    Milestones 2-3 – Demonstrate and quantify performance of advanced inverter functions standalone and in high-penetration scenarios
    Milestone 4 – Participate in development of complete test protocol

Project Results and Discussion:

The progress and findings for this project are presented here by task.

Task 1

Multi-Inverter Anti-Islanding Assessment

In FY2013, several experiments and simulation studies were done to investigate and baseline the effect of multi-inverter configurations (multiple PV inverters on one bus) had on anti-islanding performance. This involved the development of Simulink models and also hardware experiments. Tests were done on DETL's 10-node inverter testbed, and Simulink models were developed to represent the testbed and the inverters. See Figure 4.

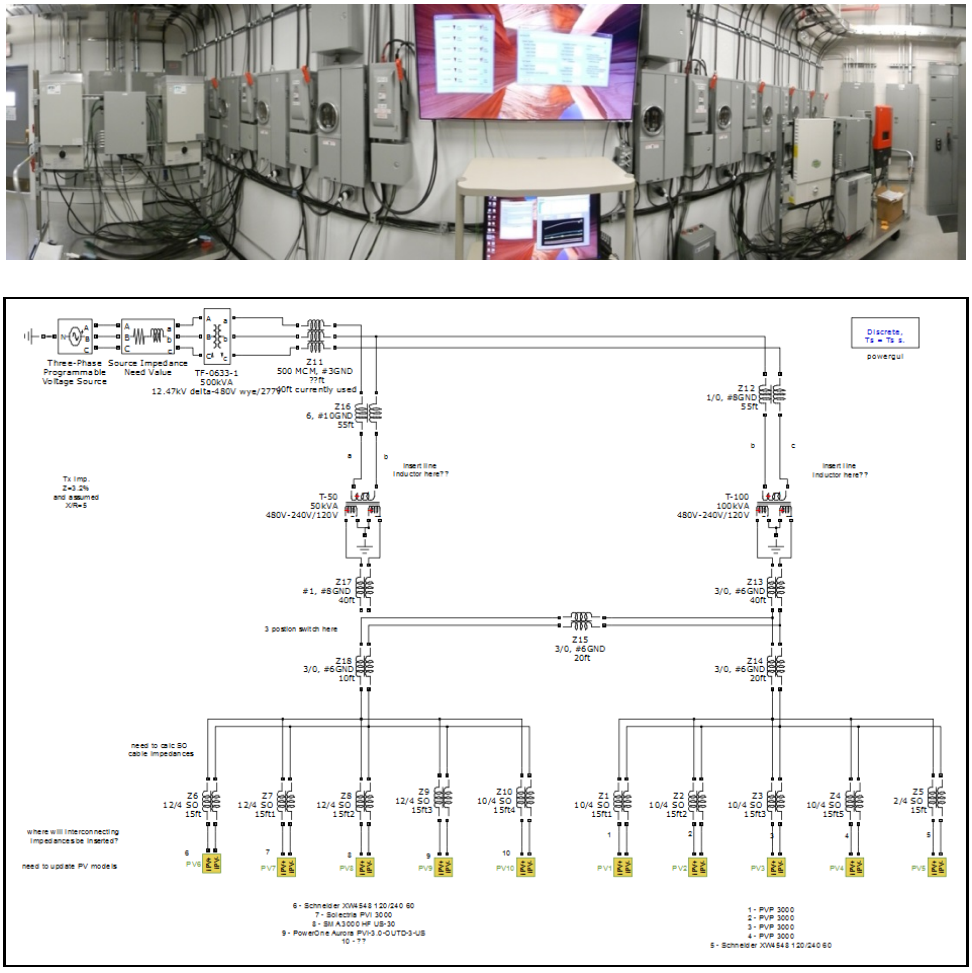


Figure 4: Photo (top) and MATLAB/Simulink model (bottom) of the DETL 10-node inverter testbed.

Several experiments were run on the physical testbed and in simulation to characterize the anti-islanding performance in terms of run-on times (ROTs) for single and multi-

inverter configurations. Figure 5 shows the comparison of a single-inverter simulation to single-inverter hardware test of ROT as a function of VAr mismatch given a real-power match. The plot shows good agreement. Figure 6 shows a simulation for a system including 1, 2, 3, 5 and 10 inverters. These results were used in the development of a SAND report [7], thus meeting a milestone for Task 1.

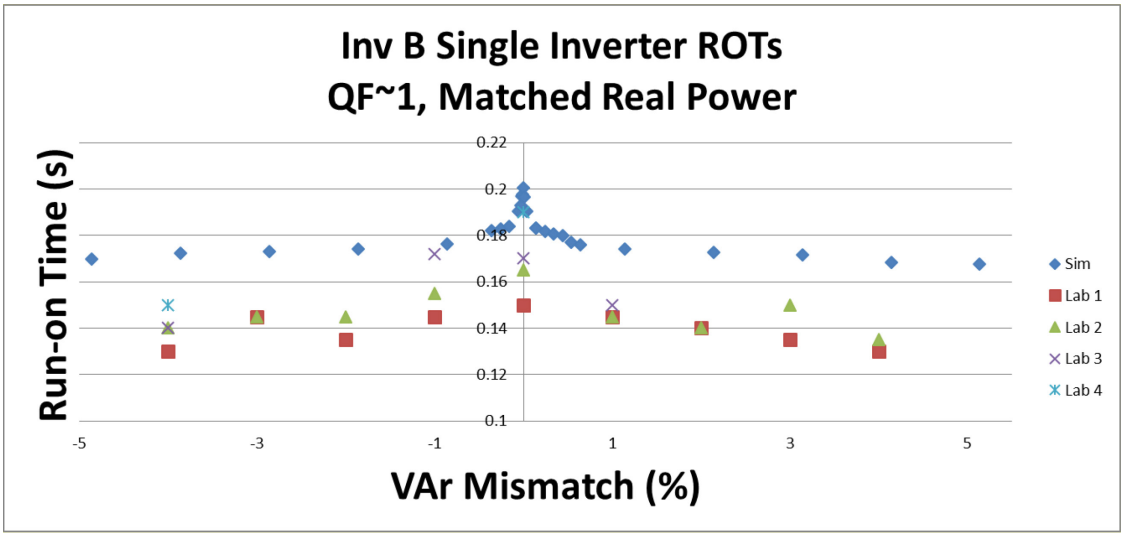


Figure 5: Simulated and measured run-on times for Inverter B, in the single-inverter case.

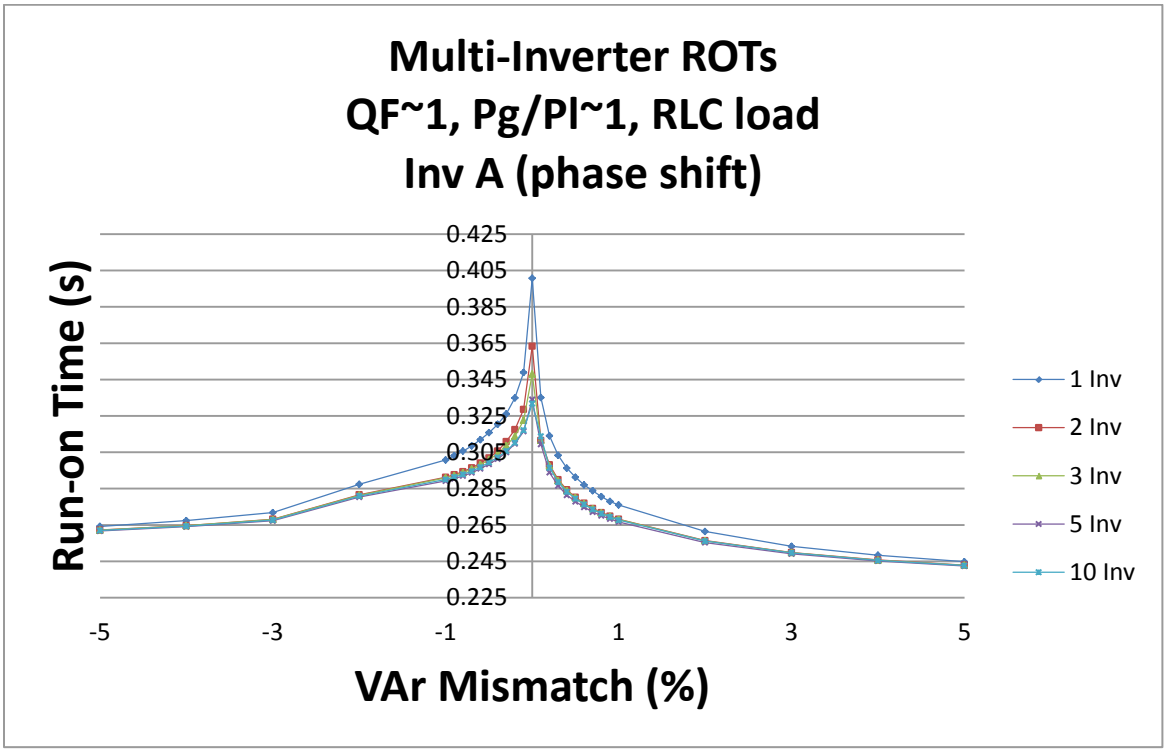


Figure 6: Simulated run-on time (ROT) vs. VAr mismatch for the phase-shift version of Inverter A. Curves are shown for islands with 1, 2, 3, 5, and 10 inverters.

In FY2014, new communications-based island detection schemes were investigated. Specifically, a new subharmonic PLC based island detection scheme was developed and tested, and evaluation of SynchroPhasor-based anti-islanding subject to time-slip was done.

PLC-based Anti-Islanding Development

To test the subharmonic PLC approach and the viability of the series injection scheme, a laboratory test was devised, test hardware was fabricated, and experimental data was taken. The experimental assembly is shown in Figure 7. The grid simulator was configured as a 120/208V 60 Hz Wye voltage source, and the subharmonic transmitter was configured to generate a 1.9 VRMS sine wave at 17 Hz in series with the a-phase of the grid simulator. The short term flicker sensation parameter *Pst* was evaluated. Starting with flicker response thresholds presented in Table 1 of [16], it was determined that a 1.34 V signal, injected on one phase of the 120/208V test circuit, would result in a *Pst* value less than 1.0 for each 120V phase voltage. However, since the receiver was measuring line-to-line voltage, the signal voltage was boosted to 1.9V. The RLC load used for islanding tests was configured for both real and reactive power match and a quality factor of 1. For this experiment, the inverter was configured such that the system islanded when the breakers were opened. Figure 8 shows the line-to-line voltage as measured by an oscilloscope at the receiver location for both the connected and islanded cases. The 17 Hz signal is nearly imperceptible in the time-domain voltage (yellow trace) but clearly present in the fast Fourier transform (FFT – red trace) of the voltage. The results were documented and published at the Applied Power Electronics Conferences (APEC2015) [34]. A provisional patent was subsequently submitted for the method [35].

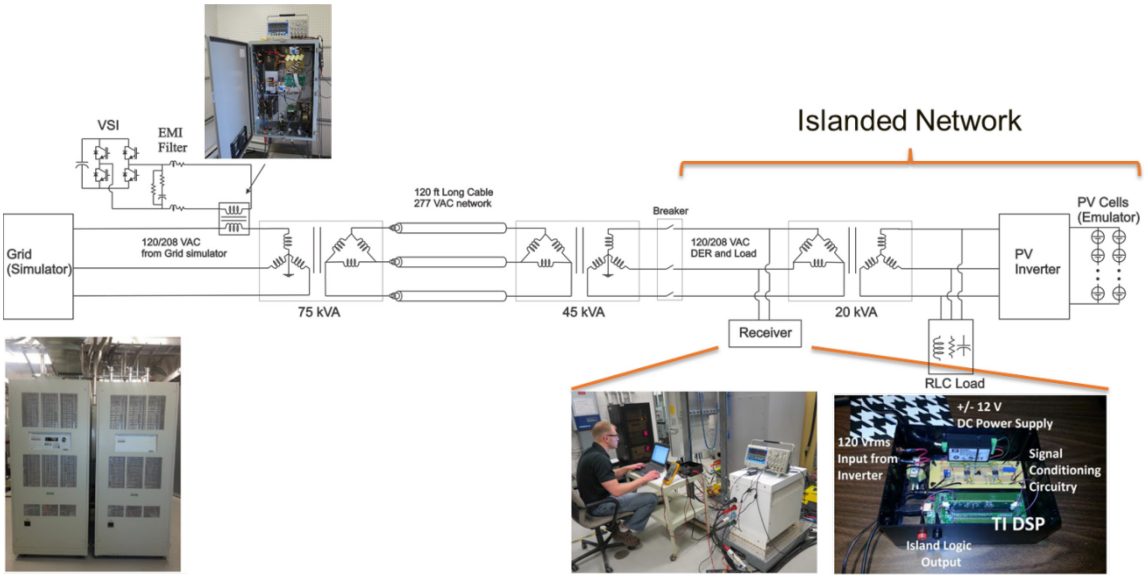
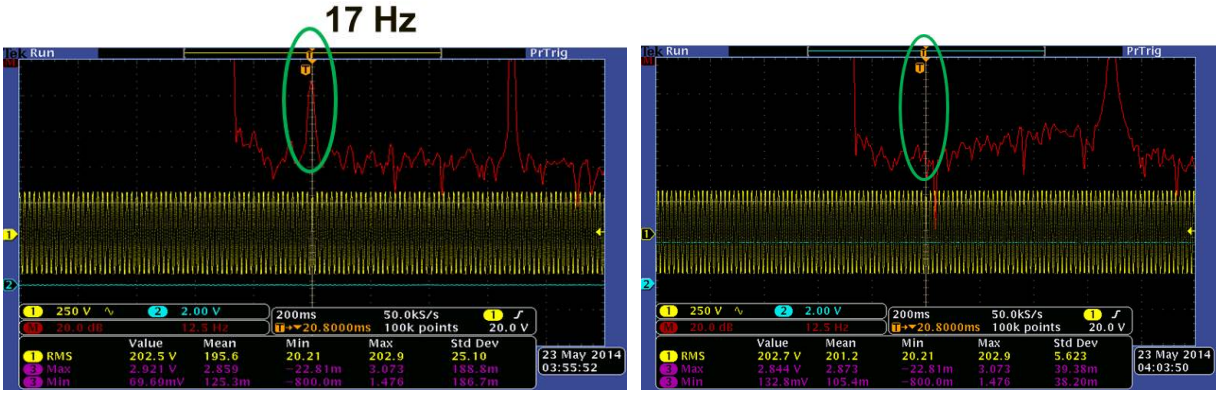


Figure 7: Laboratory setup for PLC proof of concept testing showing

Two detection Algorithms, #1 and #2, were evaluated for their islanding detection effectiveness and speed. Each algorithm was tested five times, and the detection time was recorded in each case. Detection times were measured by monitoring the utility disconnection relay signal and receiver logic output; see Figure 9. Test results are shown in Table 1. Algorithm 1 detected more quickly than Algorithm #2, largely because of the averaging window used in Algorithm #2, but both approaches were compliant with the 2 second unintentional island detection requirement stated in the IEEE 1547 standard [21].



(a) (b)

Figure 8: Line-to-Line voltage shown in time and frequency domain, measured at receiver location for (a) connected and (b) islanded

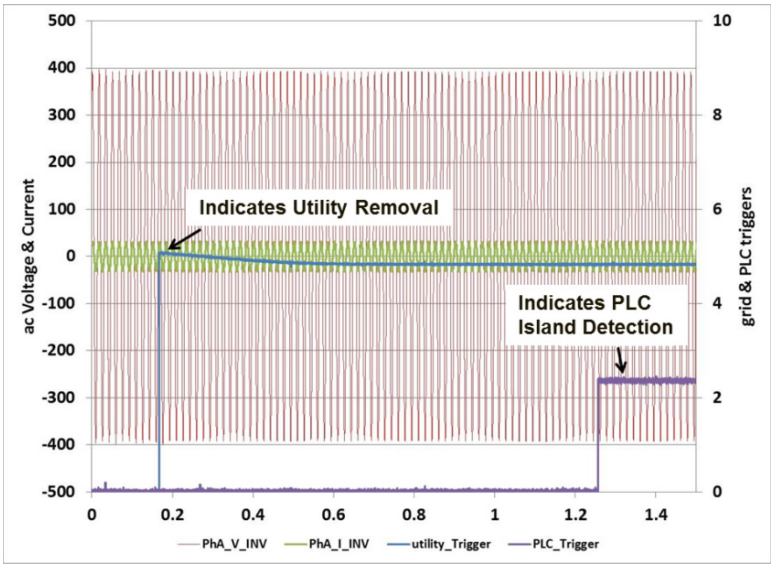


Figure 9: Waveforms from islanding test 8 showing AC line voltage, signal indicating utility removal and signal indicating island detection

Table 1: Island Detection Test Results for Algorithms 1 & 2

Test	Q factor	Pg/Pl ratio	PLC detection (seconds)
Algorithm 1 (raw signal)			
1	1	1	.386
2	1	1	.372
3	1	1	.338
4	1	1	.455
5	1	1	.418
Algorithm 2 (5 & 100ms averaging window)			
6	1	1	.574 (5ms)
7	1	1	.807 (5ms)
8	1	1	1.08
9	1	1	1.08
10	1	1	1.08

As discussed in the previous section, an FFT-based algorithm was also tested, but it did not work well due to its sensitivity to spectral leakage. When the island forms, the frequency shifts slightly off of 60 Hz, which will cause significant spectral leakage in the 60-Hz FFT. The spectral leakage causes the FFT to show a 17 Hz component even after the island forms. The FS was more immune to this because of how it was implemented.

It is noted that the dynamics of the PV inverter, which includes a perturb-and-observe style maximum power tracker, will naturally introduce some low frequency perturbations. This results in variation of the subharmonics, including 17 Hz. The measured 17 Hz component is thus expected to vary slightly. This raises the concern of false trip immunity. To test the PLCP signal integrity and attenuation, the line-to-line voltage was sampled several times in the islanded and grid-connected (grid simulator) modes of operation. Samples were taken at the receiver while islanded and connected and on the 480V circuit on the Δ-phase of the 45 kVA transformer. The magnitude of the 17 Hz component in each case was then acquired through post processing in Matlab and evaluated statistically by fitting the data to a normal distribution. Samples from the 480V circuit were scaled to be equivalent to a 120/208V circuit for easy comparison. See the histogram results in Figure 10.

When the inverter is islanded, the 17 Hz subharmonic is measured at the receiver to have a mean amplitude of 0.116 VRMS and a standard deviation of 63.7 mV. With the grid connected, the PLCP has a mean strength of 1.483 VRMS at the receiver and varies with a standard deviation of 10.3 mV. Just before the 45kVA transformer, the scaled PLCP has a mean amplitude of 1.553VRMS and standard deviation of 16.4 mV.

This indicates a mild 4.71% or 0.4 dB attenuation through the 45 kVA transformer. If the threshold for island detection were selected to be 0.75 VRMS, these results indicate that the threshold would be 71 standard deviations below the measured signal level when grid connected and 10 standard deviations above the islanded signal level, resulting in negligible false detection and negligible failed detection probabilities. This method thus shows great promise for implementation. Also, as stated above, since the method involves series voltage injection, the magnetic components of the system will be significantly smaller than those used in current injection based approaches such as the method based on that used for automatic meter reading. This development and demonstration of potential value to the utility address critical milestones for Task 1.

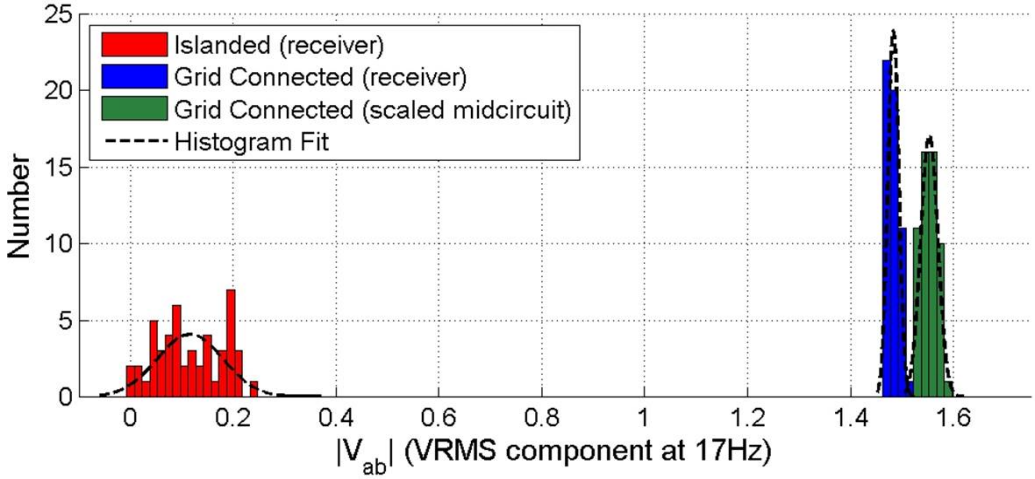


Figure 10: Histogram plot for signal strengths when islanded and grid connected

SynchroPhasor Based Anti-Islanding Evaluation

To quantify the sensitivity of three SynchroPhasor-based islanding detection methods to time slips, testing was performed at Sandia National Laboratories (SNL) in the Distributed Energy Testing Laboratory (DETL).The methods evaluated include:

- The Correlation Coefficient Based (CCB) method
- The Integral of Frequency Error (IFE)
- Frequency Slip plus Acceleration of Frequency Slip (S+A, or SpA)

In the test apparatus at the DETL, SEL-451 and SEL-487E PMUs were connected directly to a common point on the output of the DETL's grid simulator. The grid simulator allowed the use of customized frequency trajectories to help quantify the detection algorithms' time slip immunity properties. A PV inverter was also connected and was supplying power to the bus to make the test setup more realistic, although no physical island was established during testing since this was not required to meet the test objectives (i.e., this is a false-trip immunity test). Since it was impossible to purposefully initiate a time slip from the GPS output of either PMU itself, a variable delay was programmed within the SEL-3505 controller to emulate a possible time slip

between the two PMUs. In this approach, the SEL-3505 software was configured so that instead of comparing local and remote data points taken at the same time, which is the normal approach, local and remote data points taken at different times could be compared, and the behavior of the algorithm could be characterized as the local and remote data points being compared slipped farther apart in time.

To test the SynchroPhasor-based island detection scheme during a "grid event," selected events were emulated using DETL's grid simulator. Events were first simulated using General Electric's (GE) Positive Sequence Load Flow (PSLF) software. PSLF is a widely available and utilized commercial power simulation tool and is used by the Western Electric Coordinating Council (WECC), a regional reliability council, to analyze the reliability of the western North American Power System (wNAPS). WECC-developed models of the wNAPS include tens of thousands of buses and tens of thousands of components including generation, transformers, power lines, loads (linear and nonlinear), and substation equipment, and are typically developed, vetted and refined over long periods of time. Figure 11 shows a section of this PSLF model, with select components and quantities labeled.

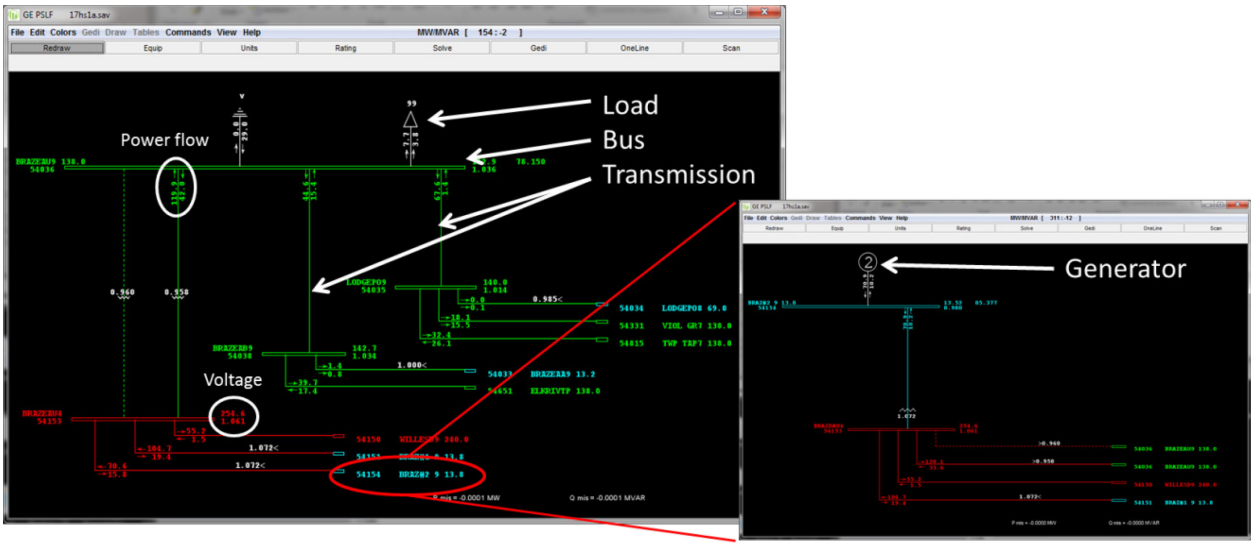
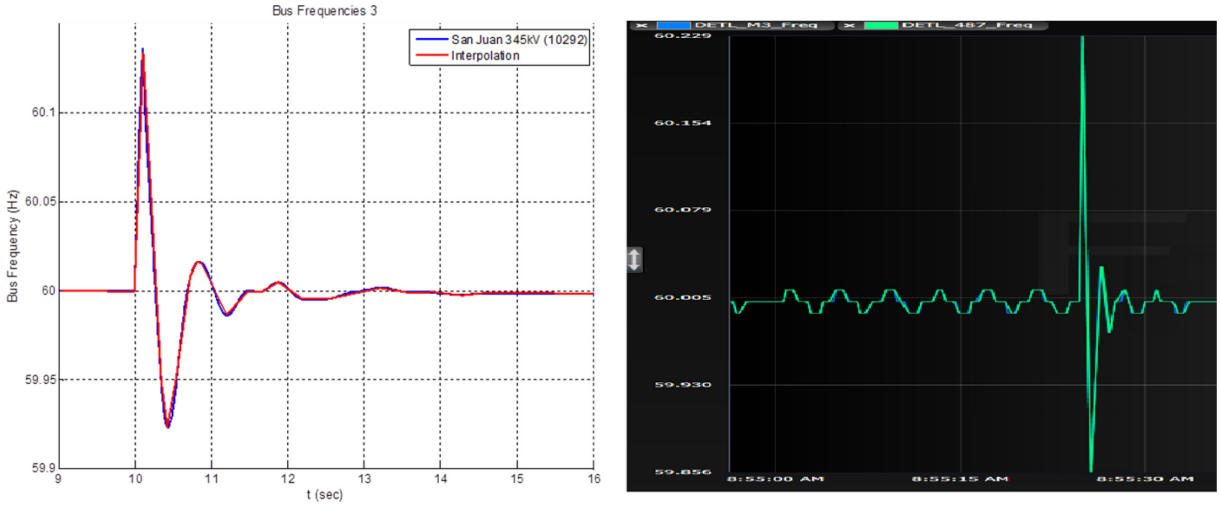


Figure 11: Screenshot from PSLF showing typical components of the wNAPS.

For this testing, the simulated frequency response on the San Juan high voltage power line during selected events was used to develop a frequency profile that could then be "played back" by DETL's grid simulator. The events selected were: (1) 100 msec fault and disconnection of a high voltage line connecting San Juan and McKinley, (2) Outage of the Palo Verde Nuclear power plant, and (3) a 500 msec Chief Joseph Brake insertion, all under the WECC's projected 2017 Heavy Summer Loading use case conditions. The first event results in a smaller and more localized disturbance, characterized as a well-damped high-frequency (~1.2 Hz) ring-down event that only lasts a few seconds. The second event results in a large frequency excursion seen

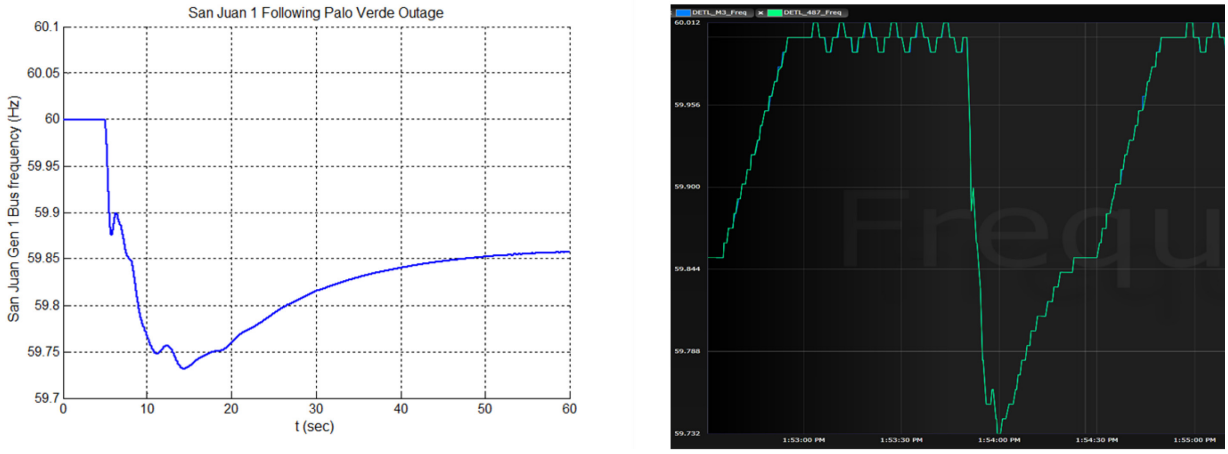
everywhere in the network and lasting nearly a minute. The third event may be regarded as a "medium event." Figure 12 shows the PSLF data plotted in Matlab, and the PMU measurement of the resulting grid simulator frequency for the first event. Figure 13 displays this information for the second event. Figure 14 displays the Matlab plot for the third event; this event was only implemented in simulation. Note that the three events are shown on different timescales.

For laboratory testing purposes, profiles 1 and 2 were implemented as a loop, so that the frequency transient repeated over and over. To avoid a discontinuity at the end of the loop, an additional ramp was added in the case where initial and final steady state frequencies were different. Also, the reader will note that there is a 10-mHz oscillation present in the grid simulator output. This was added because the grid simulator's output in steady state was 60.00 Hz and was "perfectly" constant to within the resolution of the PMUs. This is not a realistic representation of the actual grid frequency, and it also would prevent the CCB from working properly. Thus, the 10 mHz perturbations were added to emulate the non-constancy of the real grid.



(a) (b)

Figure 12: San Juan Bus frequency following McKinley line fault shown as (a) PSLF data plotted in Matlab and (b) PMU measurement of grid simulator output.



(a) (b)

Figure 13: San Juan Bus frequency following Palo Verde outage shown as (a) PSLF data plotted in Matlab and (b) PMU measurement of grid simulator output.

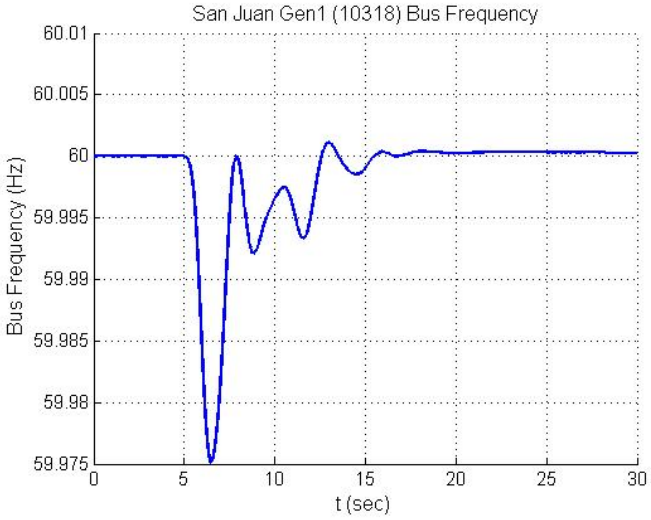


Figure 14: San Juan Bus frequency following 500 msec Chief Joseph brake insertion shown as PSLF data plotted in Matlab (this event only evaluated in simulation)

Results with Fast Transient

A summary of the DETL testing results as well as post-processing simulation results with the fast transient case (case in Figure 12) are illustrated in Table 2 for the CCB and IFE algorithms. The data show that the CCB withstood time slips of up to 3 messages, or 50 ms, without false tripping (the message rate used in the DETL was 60 msg/sec, so this also means 3 line cycles of delay). Table 2 indicates that the steady state CCB output drops as the time slip increases. When using a 512-point buffer, the CCB began to falsely trip during the fast transient at a time slip of 4 messages (67 ms). When using a 2048 point buffer, that number increased to 5 messages (83 ms) in the DETL. This

result is expected because it is already known that increasing the buffer size improves the steady state CCB output. Simulation results revealed a slightly different result when testing with a buffer size of 2048; the false trip didn't occur until a time slip of six cycles (100 ms). In this graphic, it is seen that for a time slip of five cycles and a 2048 point buffer, the simulated correlation dropped to ~80.006 when the transient occurred, which just barely missed the 0.8 threshold used to indicate an island. This result suggests that the one-cycle difference between the lab and simulation results for this particular case is probably numerical in nature, and does not indicate a fundamental disagreement between simulation and experiment.

Table 2 also indicates that the IFE proved to be considerably more sensitive to time slips—with the gains set as they presently are, the IFE would not tolerate any time slip without a false trip. In fact, there is evidence to suggest that even for a time slip of zero, the presently-used IFE gains would lead to a false trip in the fast transient case. Testing in the DETL initially showed that for a time slip of zero, no false trip occurred with the IFE method for either 512 or 2048 point buffer size. However, simulations after testing suggested that the DETL result may simply have been the result of the experiment being performed for a limited time. Figure 15 shows the simulated IFE output for two buffer sizes at a time slip of zero. Here, the IFE does in fact exceed 1 or -1 for both buffer sizes. Figure 16 shows that it takes ~80 s for a false trip to occur for the 2048 point buffer size and ~250 s for a false trip to occur with a 512 point buffer size, suggesting that had testing in the DETL been performed for a longer time, the IFE may have false-tripped during the fast transient even with a time slip of zero. To resolve this issue, the gain of the IFE algorithm may need to be reduced, an option that will be discussed shortly.

Table 2: Summary of testing results with fast transient case (transient in Figure 8).

Sandia DETL Test Results -- Fast Transient							
Slip	s.s. CCB	s.s. IFE	Buffer Size	False Trip CCB - DETL	False Trip IFE - DETL	False Trip CCB - Sim	False Trip IFE - Sim
0	~1	0.002	512	No	No	No	Yes
0	~1	0.002	2048	No	No	No	Yes
1	~1	0.004	512	No	Yes	No	Yes
1	~1	0.004	2048	No	Yes	No	Yes
4	0.97	>4	512	Yes	Yes	Yes	Yes
4	0.98	>4	2048	No	Yes	No	Yes
5	0.97	>4	2048	Yes	Yes	No	Yes
6	0.97	>4	2048	NA	NA	Yes	Yes

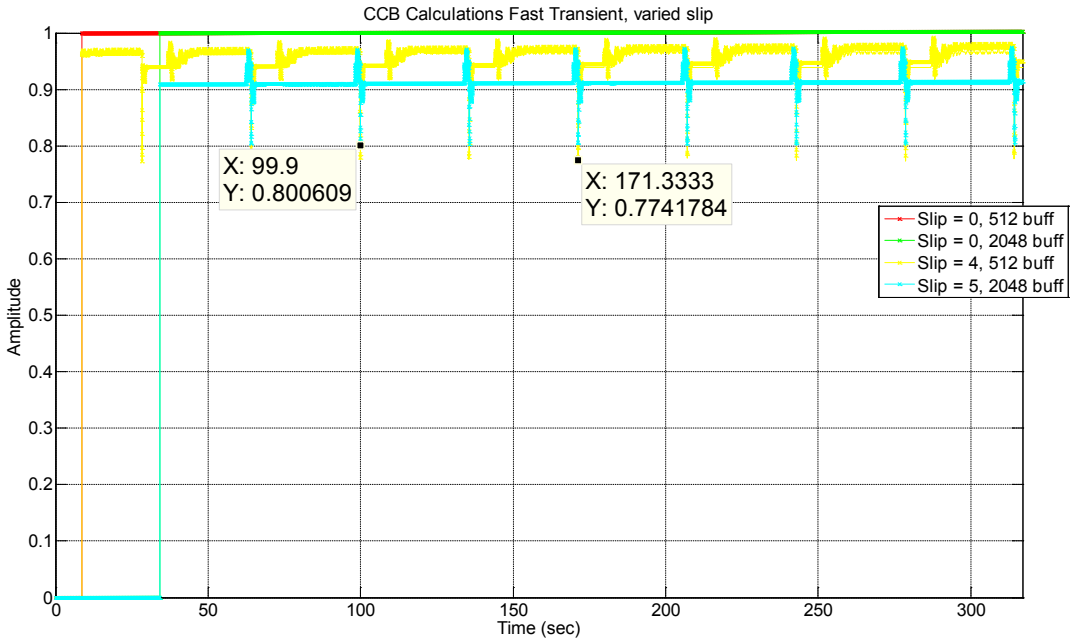


Figure 15: CCB output during fast transient event at varied time slips and buffer sizes.

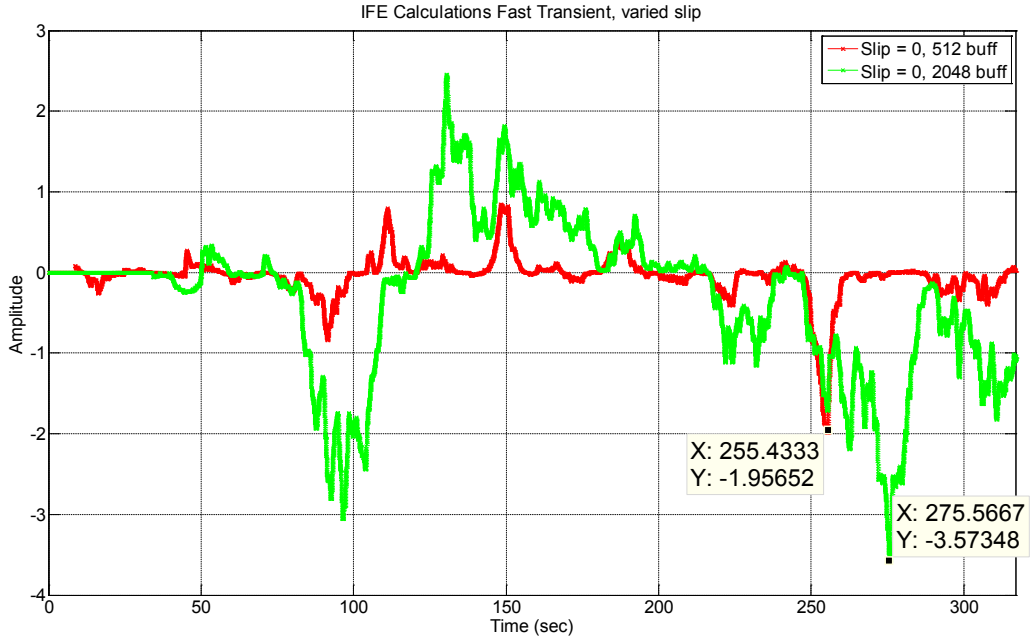


Figure 16: IFE output during fast transient event at zero time slip and varied buffer sizes.

Results with Slow Transient

A summary of the DETL testing and post-processing simulation results with the slow transient case are illustrated in Table 3 for the CCB and IFE algorithms. As with the fast transient case, the data shows that the CCB was relatively immune to time slips. During the slow transient case, a false trip in the DETL with the CCB calculated over a 512-point buffer did not occur until a time slip of ten messages (167 ms) was reached. Simulation testing suggested that, for a 2048 point buffer, no false trips occurred until a time slip of 15 messages (250 ms). Since the frequency transient used for this test was much slower than the previous case (i.e., the length of the transient is longer than the time period covered by the 512-point buffer), a longer buffer had a larger impact with regard to time slip immunity compared to the fast transient. As before, simulation results revealed a slightly different result in the DETL compared to simulation; the false trip with 512 point buffer size occurred at a time slip of nine cycles in simulation compared to ten in the DETL. The CCB simulation output for various time slips and buffer sizes are shown in Figure 17, which indicates that eventually a time slip of nine cycles and a 512 point buffer would have resulted in a false trip, and the DETL result would likely have matched the simulation result had the DETL experiment been run for a longer time period.

As with the fast transient, for the slow transient case the IFE was much more sensitive to time slips than the CCB. Testing in the DETL initially showed that for a time slip of zero, no false trip occurred with the IFE method for when using a 512 point buffer (testing at 2048 points wasn't tested in the DETL). However, similar to what was reported for the fast transient case, simulations after testing (shown in Figure 18) revealed that the IFE does in fact exceed 1 or -1 for both buffer sizes, for a time slip of zero, but only after ~150 s. Thus, it is again hypothesized that testing in the DETL would have revealed an IFE false trip at a time slip of zero had the experiment been run longer. To resolve this issue, the gain of the IFE algorithm may need to be reduced, which will be discussed shortly.

Table 3: Summary of testing results with slow transient case (transient in Figure 9).

Sandia DETL Test Results -- Slow Transient							
Slip	s.s. CCB	s.s. IFE	Buffer Size	False Trip CCB - DETL	False Trip IFE - DETL	False Trip CCB - Sim	False Trip IFE - Sim
0	~1	0.002	512	No	No	No	Yes
0	~1	0.002	2048	NA	NA	No	Yes
1	~1	0.004	512	No	Yes	No	Yes
5	0.99	>6	512	No	Yes	No	Yes
8	0.951	>10	512	No	Yes	No	Yes
9	0.94	>10	512	No	Yes	Yes	Yes
10	0.93	>10	512	Yes	Yes	Yes	Yes
15	0.89	>10	2048	NA	NA	Yes	Yes

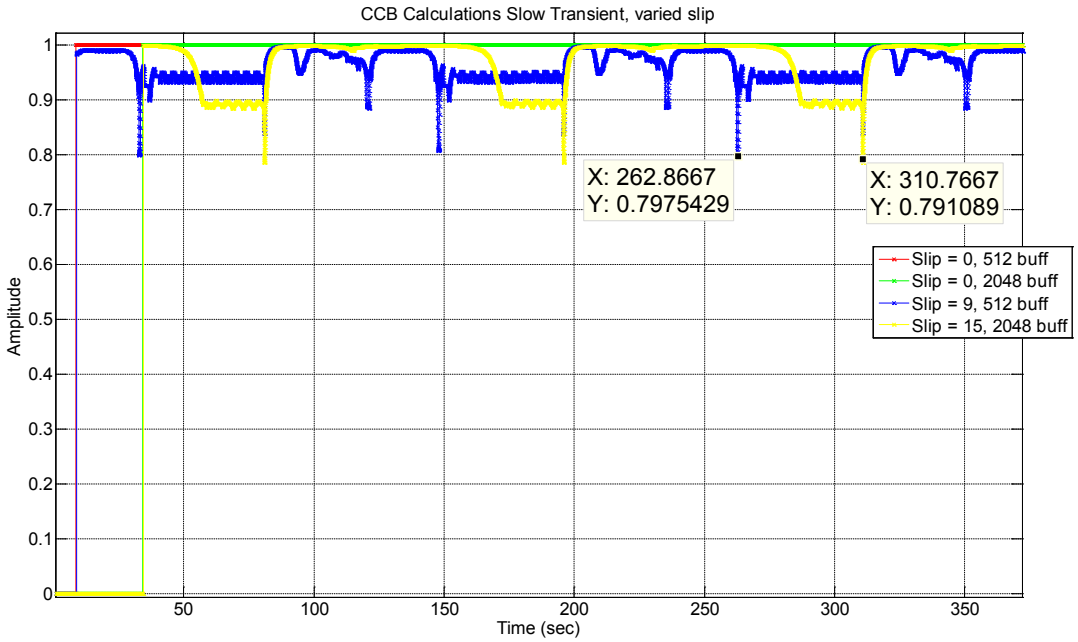


Figure 17: CCB output during slow transient event at varied time slips and buffer sizes.

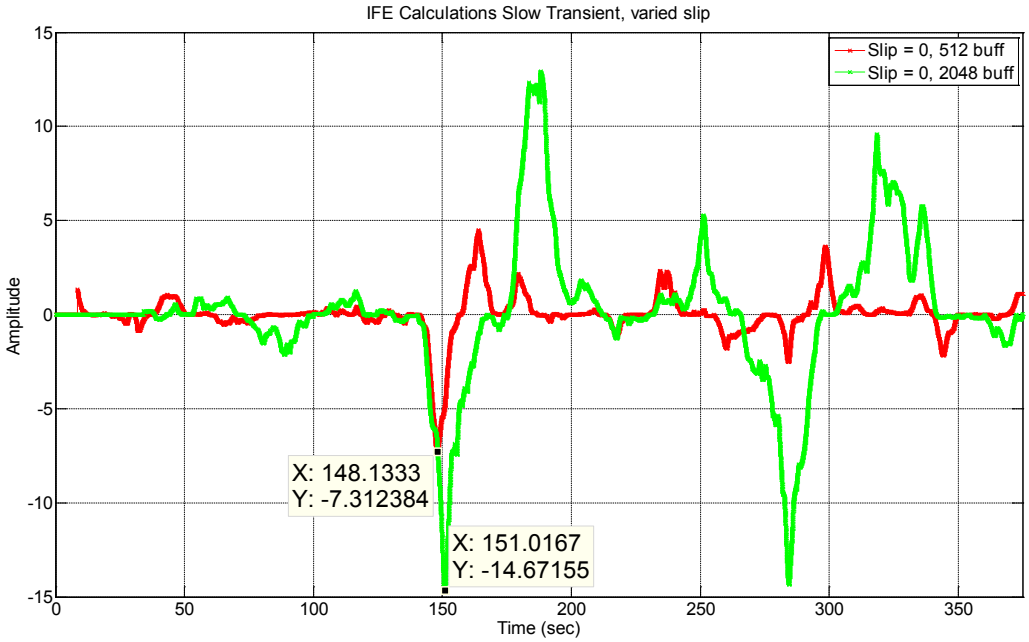


Figure 18: IFE output during slow transient event at zero time slip and varied buffer sizes.

Results with Medium Transient

The medium transient case, event 3, was only evaluated in simulation. The results are summarized in Table 3. In summary, the IFE failed after 1 cycle slip and CCB failed after 9 cycles of slip. However, for this particular transient the S+A method never false tripped. This could be caused by 2 factors, (1) the data came from simulation and not from a PMU, which would add non-idealities numerically or (2) the amplitude of the transient is only 25 mHz, and doesn't result in a significant enough slip+accel deviation to cause a false trip to occur.

Table 3: Simulation results with medium transient case (transient in Figure 10).

Simulation Test Results -- Medium Transient				
Slip	Buffer Size	False Trip CCB - Sim	False Trip IFE - Sim	False Trip S+A - Sim
0	512	No	No	No
1	512	No	Yes	No
9	512	Yes	Yes	No
100	512	Yes	Yes	No

Although additional scenarios were studied and documented (with plots and tabulated results), for the sake of brevity, they are not included in this report.

Task 2

In this task, work was done to evaluate the efficacy of anti-islanding schemes in single-inverter and multi-inverter configurations, with and without advanced inverter functions. In addition, a collaborative controls method is developed and compared in simulation. Results of experimental work are also discussed.

Collaborative Controls Development

A new collaborative controls approach was devised using the islanding test reference model developed in FY2013. See Figure 19. The approach is an augmentation of the Sandia Frequency Shift (SFS) method and applies a time-scale separation to the frequency/watt function (ie a filter) through selection of τ_{FW} to avoid interaction between the GSFs and the positive feedback of the SFS approach. Thus, during a disconnection, the freq-volt trajectory will not be inhibited over short time scales. Selection of a voltage filter coefficient τ_{VV} may be applicable in future applications but was not investigated here.

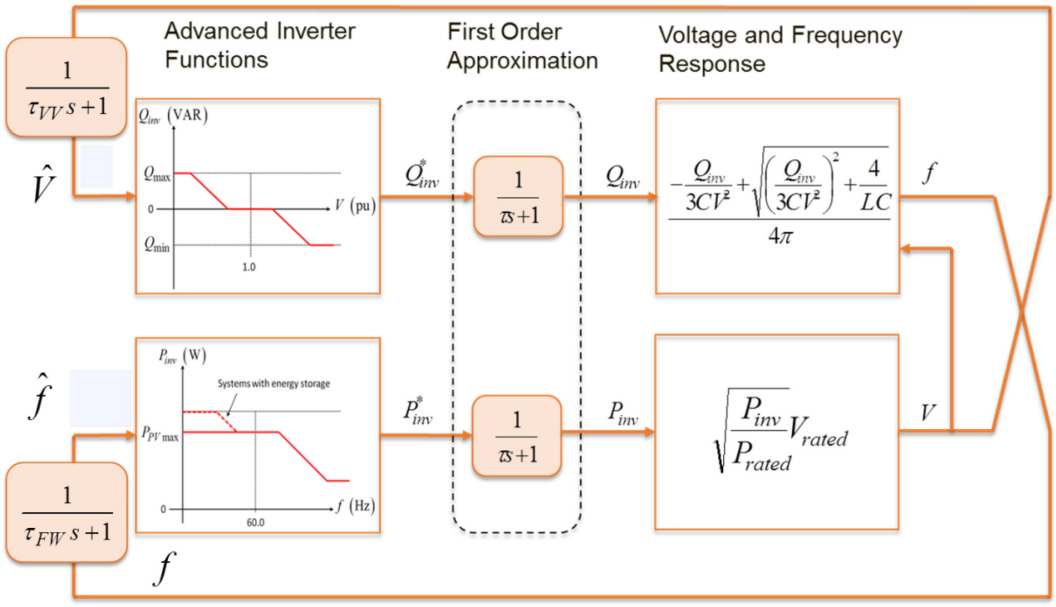


Figure 19: Anti-Islanding Reference Model for Islanding Test with GSFs

The operation of the control is distinguished in Figure 20. The inner red dotted line indicates the current 1547 voltage and frequency trip points. The outer red dotted line indicates potential new voltage and frequency trip points given V/FRT. Therein, Figure 20a shows the frequency-voltage trajectory for a system with matched source and load and no active anti-islanding. It is noted for this case the trajectory is stable within limits and that the system would not trip. In Figure 20b, the SFS is implemented and a slightly positive frequency error results, through positive feedback, in a trajectory that violates the frequency constraints, and the system is expected to shut off. In Figure 20c, the SFS and GSFs are implemented on the converter and the negative and positive feedbacks cancel one another, resulting in a stable trajectory; this system would continue to run on. In Figure 20d, the time scale separation is implemented. The trajectory moves left outside the box, violating the frequency constraint. Given enough time, the trajectory would return back to the inside of the box, but because of the time-scale separation, the GSF and SFS do not interact in the short time span following a grid disconnection. This implementation would accomplish both the grid support objectives and robust anti-islanding.

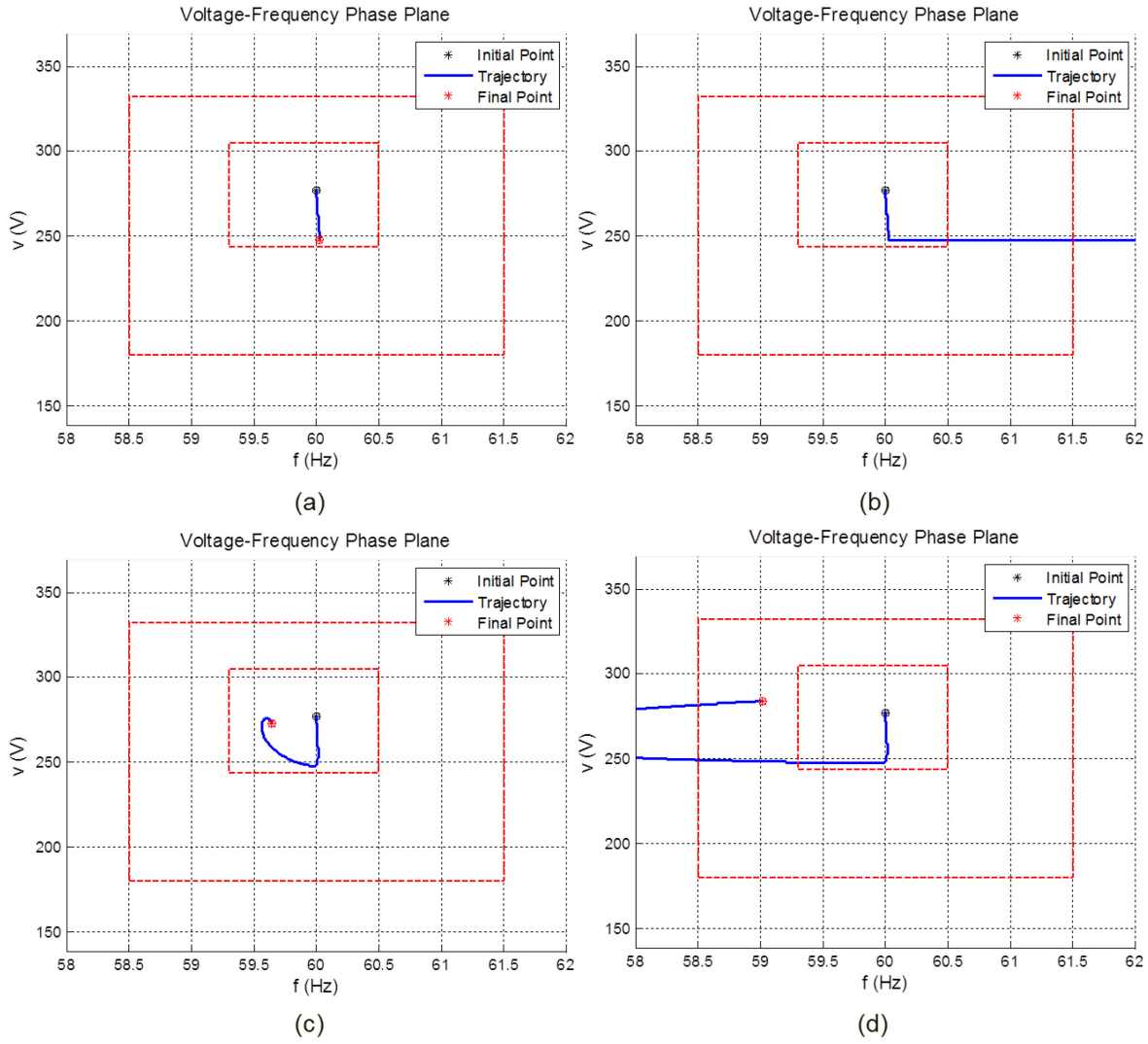


Figure 20: Frequency-Voltage Trajectories predicted by Reference Model for (a) Passive Anti-Islanding only OUV/OUF, (b) Active Anti-Islanding SFS (positive feedback), (c) SFS with Grid Support Functions, and (d) SFS and Grid Support Functions with Time Scale Separation

Figure 20 only illustrates a single scenario with different control schemes. To illustrate the function's efficacy over a larger set of scenarios, islanding maps were generated for different cases using Sandia-developed generic inverter models. These are shown in Figure 21. In each, a red square indicates a failure to detect an island in 2 seconds, green triangles indicate an under-frequency trip, green circles indicate an over-frequency trip, blue cirucle indicate an over voltage trip, and blue triangles indicate an under voltage trip. Figure 21a shows the results for SFS, indicating no non-detection zone (NDZ) visible. In Figure 21b, results are shown for the addition of GSFs, and a small NDZ is present. In Figure 21c, the voltage and frequency ride throughs were added, increasing the size of the NDZ. Finally, in Figure 21d, the collaborative controls

were implemented with voltage and frequency ride throughs, and the NDZ is no longer visible. This generalizes the result indicated in Figure 20.

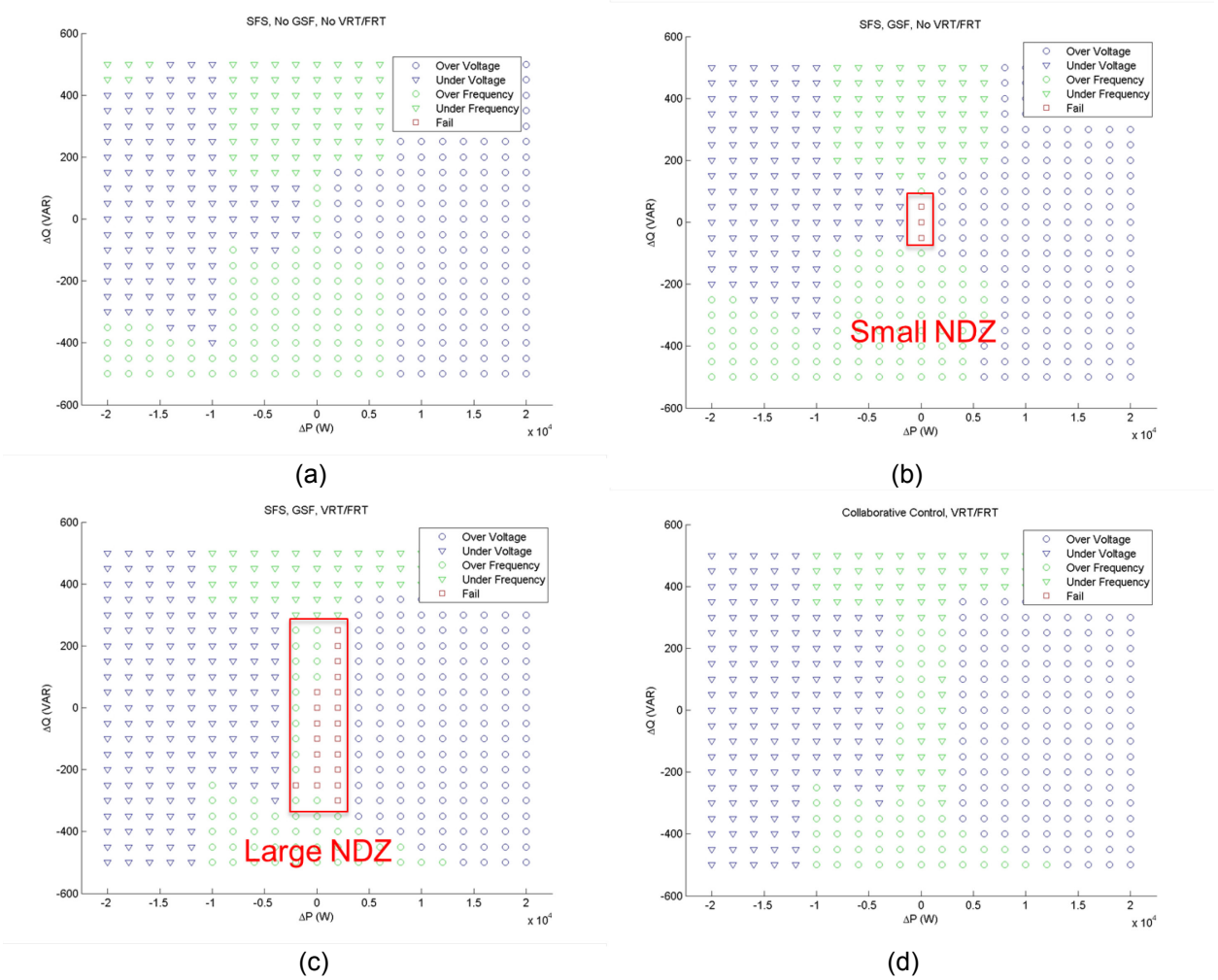


Figure 21: Islanding Maps predicted by Reference Model for (a) Anti-Islanding SFS (positive feedback), (b) SFS with Grid Support Functions, (c) SFS with Grid Support Functions and V/F RT, and (d) Collaborative Controls with V/F RT

Multi-Inverter Simulations in Simulink with and Without GSFs and V/FRT

MATLAB/Simulink simulations have been run using a detailed model of a 3 kW residential single-phase inverter to attempt to quantify the impact of grid support functions on islanding detection effectiveness. This inverter utilizes an anti-islanding method that falls within the general family of impedance detection-based methods. The intent of this work was to examine the impact on impedance detection-based islanding detection of the addition of low voltage ride through (LVRT), low frequency ride through (LFRT), and volt-VAr and frequency-Watt functions, collectively referred to herein as “grid support functions” (GSFs).

Simulations were run in a three-phase testbed. The 3 kW inverter is a single-phase device, so three were used, one per phase, connected in delta and interfaced to the

testbed feeder through a Yg-Yg distribution transformer. Simulation batches were run without any of the GSFs, to establish an anti-islanding baseline, and then with GSFs enabled, to see what impact adding them has. For each simulation, the load power and the island VAr balance (P and Q mismatch within the island) were swept over ranges, and the run-on times (ROTs) at each load P vs. ΔQ pair were recorded and plotted. Simulations were run at three irradiance levels: 0.33 kW/m^2, 0.66 kW/m^2, and 1 kW/m^2. The length of these simulations is such that the longest ROT that can be detected is 5 s. This was chosen because the nature of this system is such that if detection does not occur within that time, it is because the system has reached a sufficiently stable state that it will never detect. Thus, in the results that follow, a 5 s ROT can be taken to be an indefinite ROT.

Figure 22 shows two surface plots of the ROT versus VAr and watt mismatch, for the case of 33% irradiance. At first, the result is quite surprising: addition of the GSFs unquestionably *improved* the islanding detection effectiveness of the Z-detection inverter. In the left-hand plots (no GSFs), there is a broad range of 5 s, and thus indefinite, ROTs, occurring over a fairly wide range of load powers and a narrower range of VAr mismatch values. However, when the GSFs are activated, the ROTs are reduced in essentially all cases, and the large region of elevated ROTs in the left-hand plots are gone, replaced by a few individual isolated elevated points.

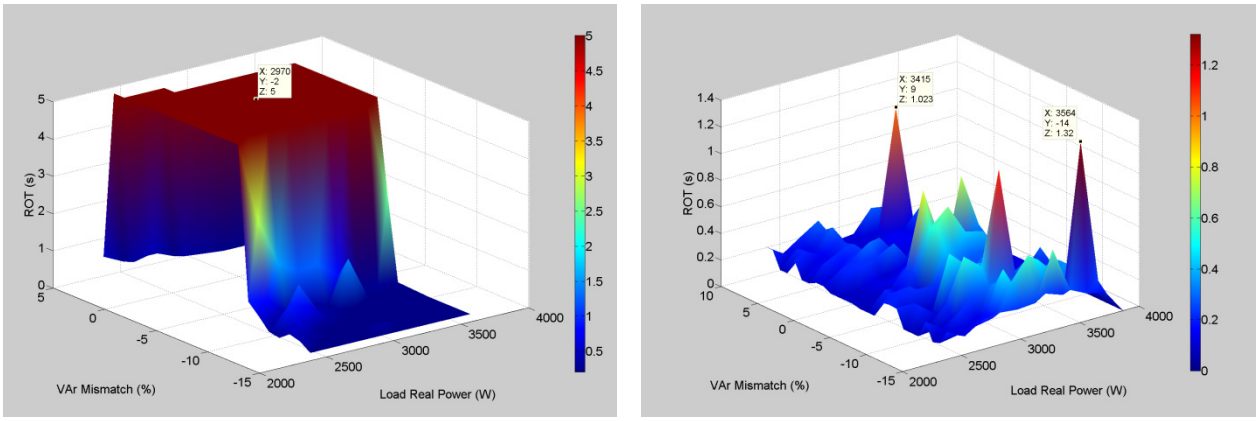


Figure 22. Results for 33% irradiance, surface plot view. Left: GSFs off. Right: GSFs on.

Figure 23 shows two surface plots of the ROT versus VAr and watt mismatch, for the case of 66% irradiance. The results are similar to the 33% irradiance case in that the activation of the GSFs significantly improved the ability of the inverter to detect islands, and ROTs dropped in nearly all cases. Note that the extent of the NDZ in the no-GSF case is somewhat smaller at the higher irradiance level.

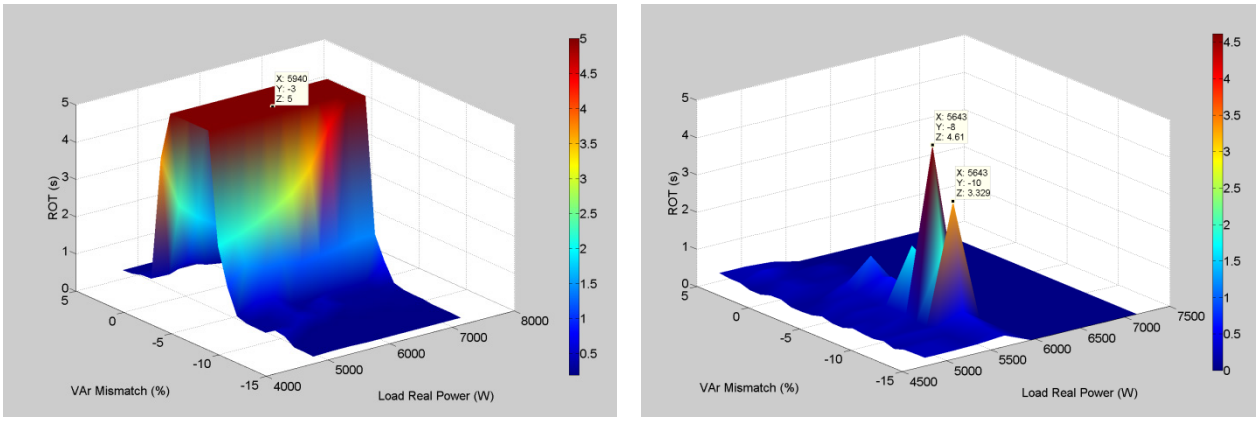


Figure 23. ROTs vs. P and Q mismatch for 66% irradiance. Left: no GSFs. Right: GSFs active.

Figure 24 shows two surface plots of the ROT versus VAr and watt mismatch, for the case of 100% irradiance. Again, the results are similar; activation of the GSFs has reduced the NDZ. However, two interesting trends are apparent. One is that the original NDZ in the no-GSF case is smaller for 100% irradiance than for 66%. The other is that the amount of improvement obtained by activating the GSFs is smaller, as indicated by the fact that the NDZ with the GSFs on is closer in size to the no-GSF NDZ than was the case at either of the lower irradiance levels.

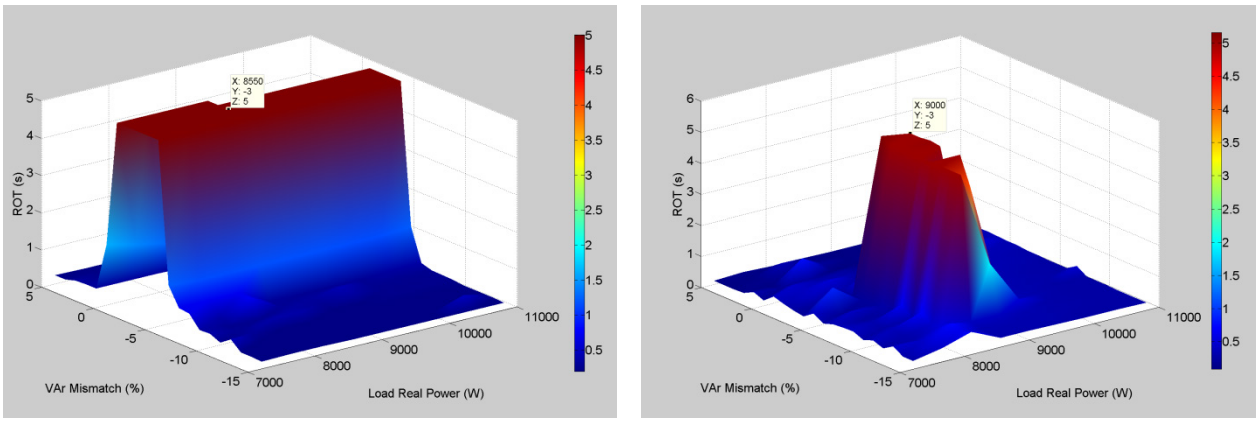


Figure 24. ROTs vs. P and Q mismatch for 66% irradiance. Left: no GSFs. Right: GSFs active.

It was expected that ROTs for an impedance-detection method in a single inverter case would be minimally impacted by the presence of GSFs. Impedance detection, particularly the pulse-based variety, actively disrupts the island's ability to come to a steady state, and unless something in the implementation of the GSFs causes the impedance detection pulse to change in magnitude or duration, that disruption of the steady state should persist even when GSFs are active. It would also be a fairly simple matter to have the impedance detection pulse "ride on top of" the output variations required by the GSFs. However, there were two results seen here that were somewhat surprising.

The first was that in the baseline case, with no GSFs but with three single-phase inverters connected in delta, a fairly large NDZ was observed. This was not expected based on past testing with this inverter. It is believed that the primary reason for the NDZ lies in the fact that three inverters with non-synchronized impedance detection AI are used, and are in a delta configuration. The fact that they are connected in delta but the loads are in Y means that the dV/dI seen by each inverter is not caused only by that inverter, and thus the level of correlation between V and I is reduced, leading to a lessened ability of the inverters to see island formation. The second surprising result was that addition of the GSFs actually improved the islanding detection effectiveness of the PV plant. It is believed that this improvement occurs because, when the system is islanded, there is coupling between V, f, P and Q, such that the volt-VAr and frequency-watt functions actually slightly destabilize the island. Consider an island that is slightly deficient in watts but well-balanced in VArs. When the island forms, the voltage falls because of the power deficit. The volt-VAr functions become active, and the inverter begins to source VArs to attempt to support the voltage. However, while the voltage may rise somewhat, the island will now be VAr-rich, and there may not be an operating point at which the load's VAr demand and the PV's volt-VAr curve are both satisfied. Thus, the system begins "hunting" and cannot reach a stable steady state. Similar situations will occur for islands that are slightly power-rich, or slightly VAr-rich. In a VAr-deficit island, one would expect less of an impact of this cross-coupling because of the asymmetry of the frequency-watt function.

Collaborative Controls Simulation in Simulink

Efforts were made to incorporate collaborative controls into the transient model of a commercial inverter (referred herein to as inverter A). The model has the following blocks built into it: hardware components including DC and AC filters and switch averaged bridge, generic PV array model using a controllable voltage source and series impedance with irradiance as an input, MPPT, four standard relay blocks with user programmable trip settings, active anti-islanding logic, DQ based current controls with decoupling logic, and grid support functions (VV and FW) with user programmable settings. A screenshot of the Simulink model is shown in Figure 25.

The simulation plots shown below were prepared by Northern Plains Power Technologies in collaboration with Sandia and with the inverter manufacturer; these show surface plots and histograms depicting the run-on times (ROTs) following utility disconnect. Figure 26 shows the ROTs for several VAr and real power mismatches in the baseline configuration of 100% irradiance, no GSFs, 1547 trips; peak ROT is around 0.35 sec. Figure 27 shows the same with grid support functions (GSFs) turned on; little to no degradation is noted in the anti-islanding performance.

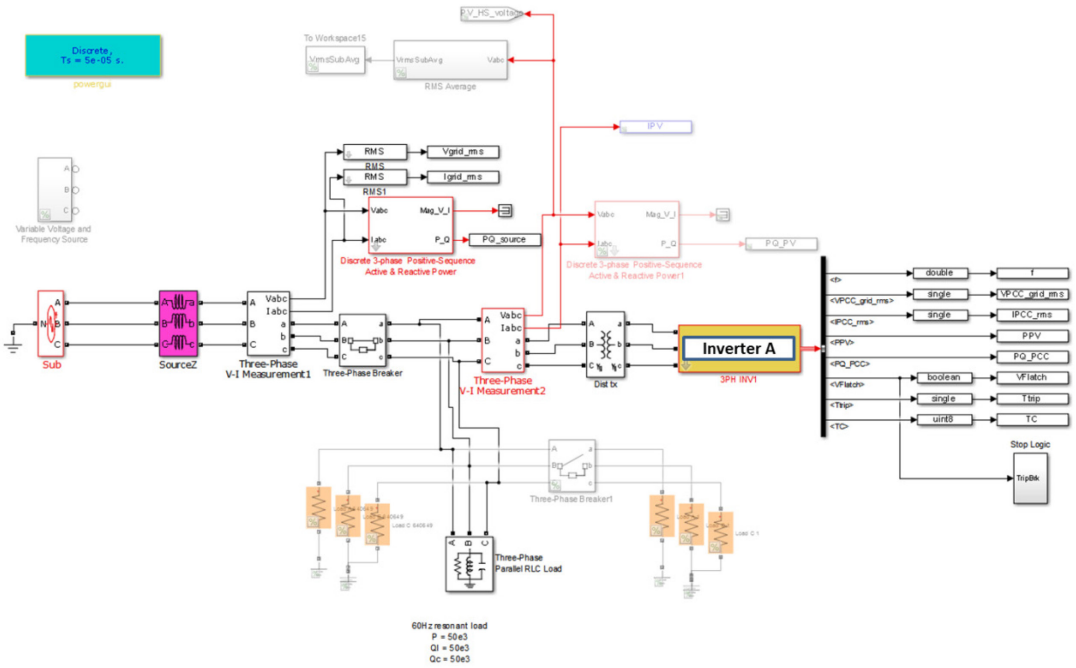


Figure 25: Screenshot of Inverter A model being developed in Simulink

As seen in Figure 28, initiating the new 1547A relay settings results in increased peak ROTs. In Figure 29, the converter implements SFS with GSFs and 1547A relay settings with Watt priority. The ROTs are seen to approach 1 sec at several operating points. The differences in performance seen in Figures 28 and 29 are due to the inverter hitting a real or reactive power limit which causes shifts in the P-Q balancing in the island that in turn causes either V or f to trend out of spec at a different rate than without hitting limits. The Sandia-NPPT team is currently evaluating the specifics of this in the context of the reference model.

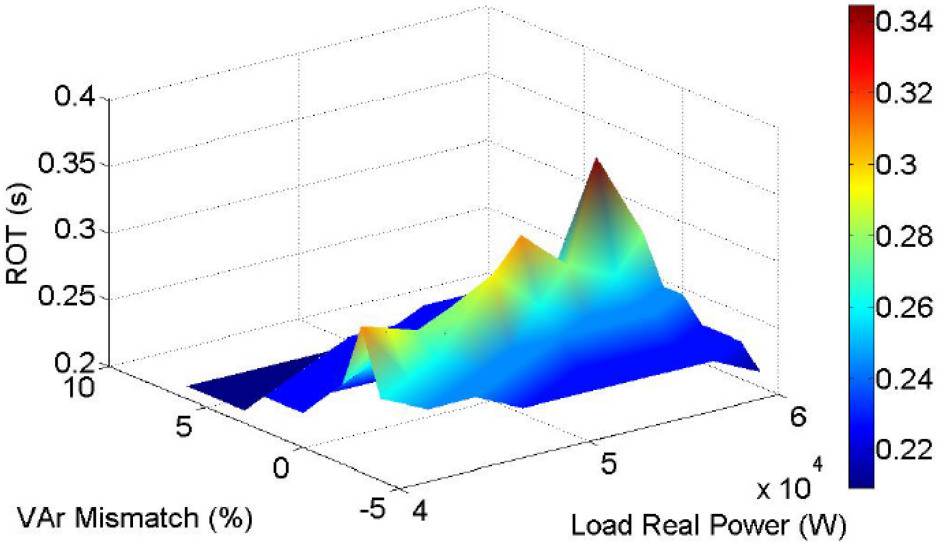


Figure 26: ROTs for SFS, Irradiance =100%, GSFs Off, 1547 relays

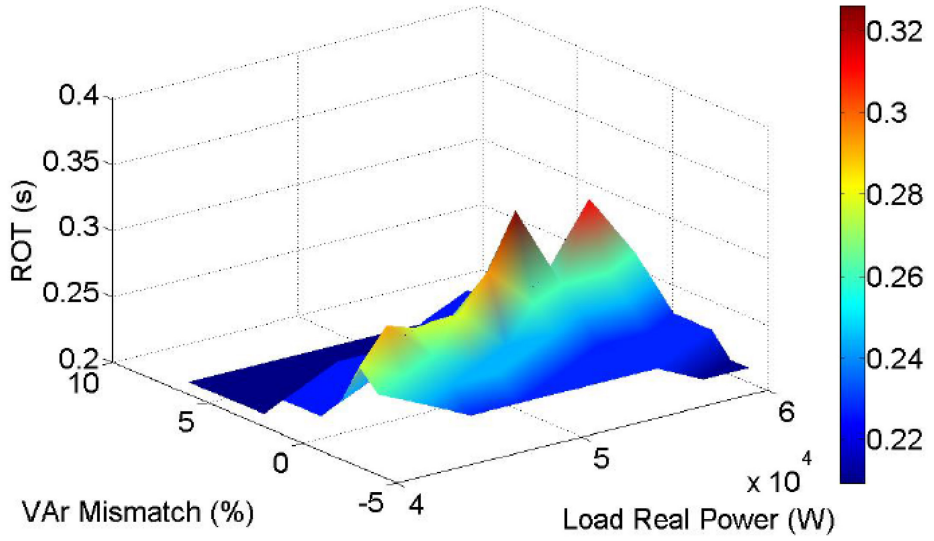


Figure 27: ROTs for SFS, Irradiance =100%, GSFs On, 1547 relays

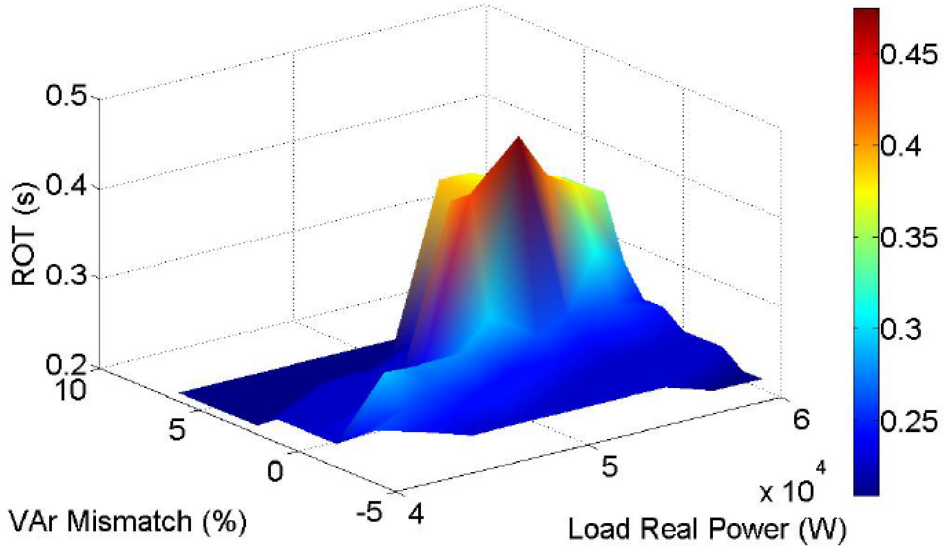


Figure 28: ROTs for SFS, Irradiance =100%, GSFs On, 1547A relays (VAr priority)

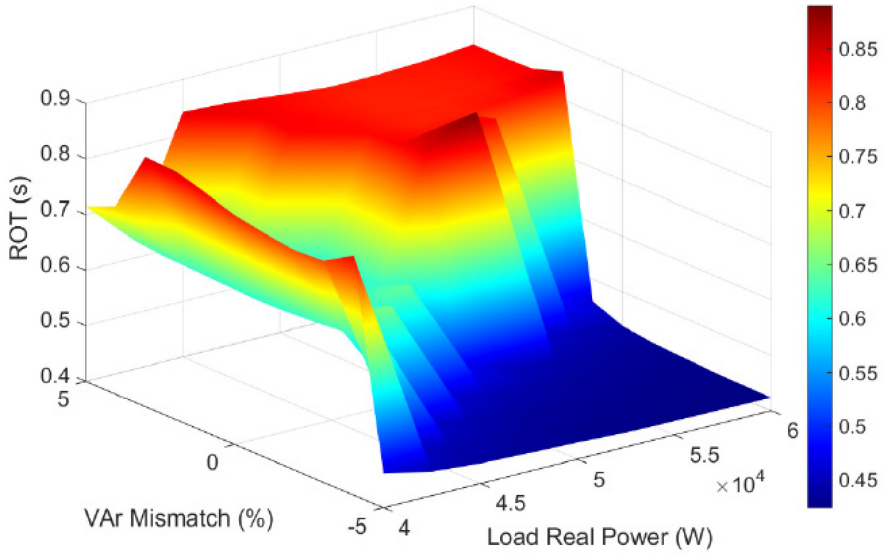


Figure 29: ROTs for SFS, Irradiance =100%, GSFs On, 1547A relays (Watt priority)

By cumulating the results over a surface, it is possible to generate a histogram of ROTs for a particular operating condition. Figure 30 shows the results of the same conditions reported in Figure 29 with and without the collaborative control filter. In this case, it is noted that a collaborative control filter with a 2 sec cut off frequency reduced the peak ROT from nearly 1 second to below 0.5 seconds, thus improving the anti-islanding performance considerably while implementing grid support functions and new 1547A relay trip points.

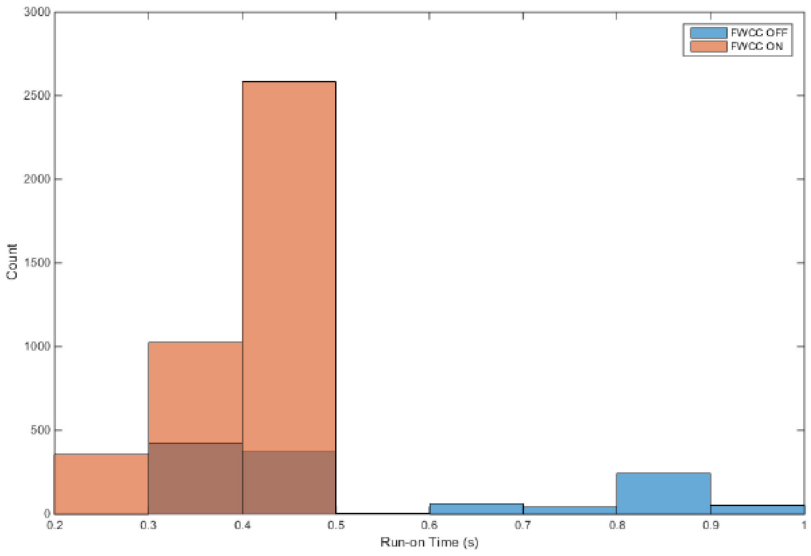


Figure 30: Comparing SFS at 100% irradiance with frequency-watt, 1547A trips, with and without collaborative controls

Collaborative Controls Experiment

The Sandia team engaged the manufacturer of Inverter A for the implementation of the collaborative controls scheme. Inverter A was a 50kW 3-phase PV inverter containing an isolation transformer that connects to a 480Vac bus. The inverter utilizes an Active Frequency Drift (AFD) or alternatively a Sandia Frequency Shift (SFS) depending on the implementation. The frequency measurement used for both the AFD and for the frequency-watt function is taken from the phase-locked loop (PLL) frequency state estimate. This estimate converges to the real frequency at a high rate. Sandia proposed that a separate filtered frequency be used for the frequency-watt function to avoid interaction between the AFD and the negative feedback of the frequency-watt functions. The manufacturer dedicated an engineer to the task who worked onsite with the Sandia team to implement the approach. With the limited tests performed, the results were inconclusive but they are summarized here.

Preceding the work to implement the collaborative controls, the Sandia team supported the manufacturer in the implementation of their frequency-watt function; see Figure 31. After the freq-watt, volt-VAr, L/HVRT and L/HFRT capabilities were verified with the grid simulator, four tests were conducted with the following results:

1. Real power match at 30 kW, LC adjusted for zero reactive power and quality factor of 1, advanced functions disabled, AFD anti-islanding scheme enabled. An island was detected when the utility disconnected, and the inverter ceased to deliver power.
2. Real power match at 30 kW, LC adjusted for zero reactive power and quality factor of 1, advanced functions included freq-watt, volt-VAr, L/HVRT and L/HFRT were enabled, AFD anti-islanding scheme enabled. The inverter islanded indefinitely indicating an interaction between the AFD and advanced functions prohibiting an island detection. See Figure 32.
3. Real power match at 30 kW, LC adjusted for zero reactive power and quality factor of 1, advanced functions included freq-watt, volt-VAr, L/HVRT and L/HFRT were enabled, AFD anti-islanding scheme enabled, and a filter was added with τ_{FW} = 3.14 sec (2 Hz bandwidth) between the PLL and freq-watt function. An island was detected within approximately 0.7 sec when the utility disconnected, and the inverter ceased to deliver power. See Figure 33.
4. Real power match at 30 kW, LC adjusted for zero reactive power and quality factor of 1, advanced functions included freq-watt, volt-VAr, L/HVRT and L/HFRT were enabled, AFD anti-islanding scheme enabled, and the filter was disabled. This test is essentially a repeat of test 2. The inverter islanded indefinitely.

Unfortunately, the results are inconclusive because test 3 was only run once, and there is evidence of a slight LC mismatch, which in previous tests shows the AI stopping the island within the 2 seconds. Sandia team attempted to coordinate more testing with the

manufacturer in Q2 and Q3, but the financial status of the company prevented technical support on this effort, which led to limited testing.

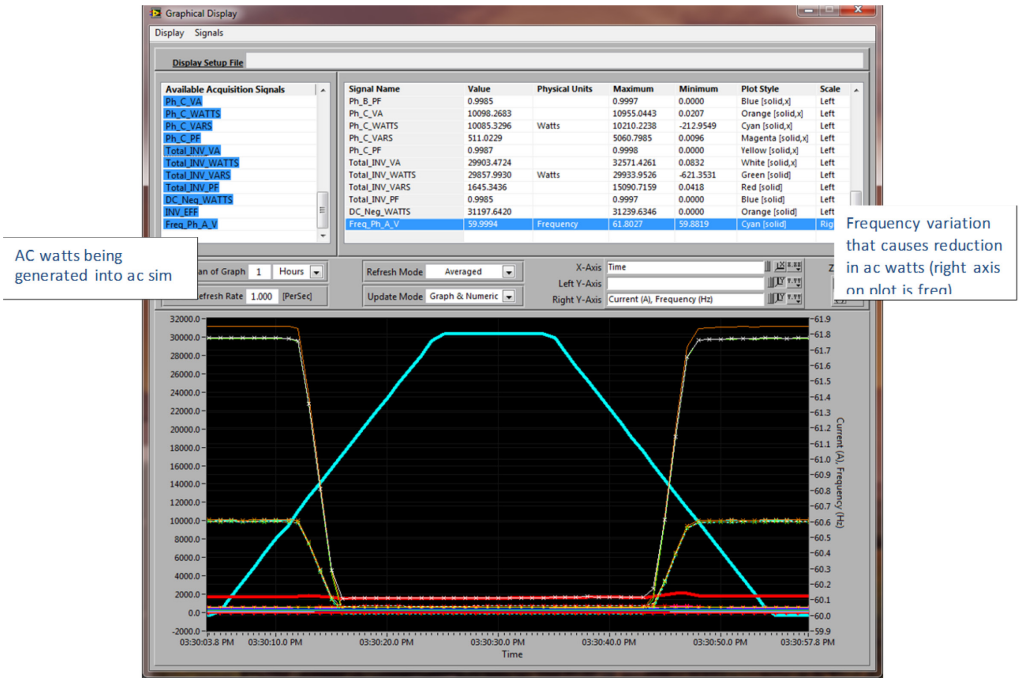


Figure 31: Screenshot of grid simulator test verifying the freq-watt implementation

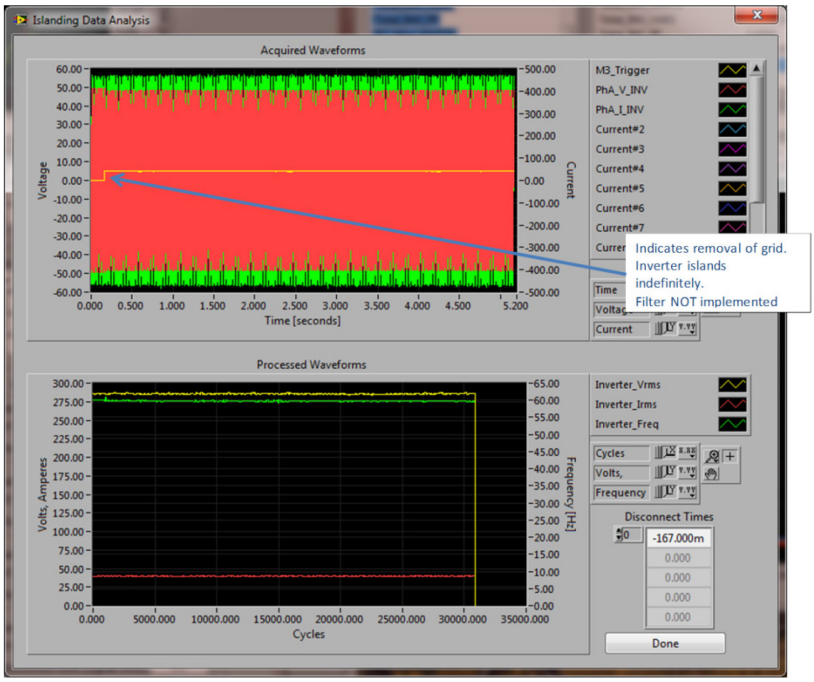


Figure 32: Screenshot showing indefinite run-on during islanding test (Test 2)

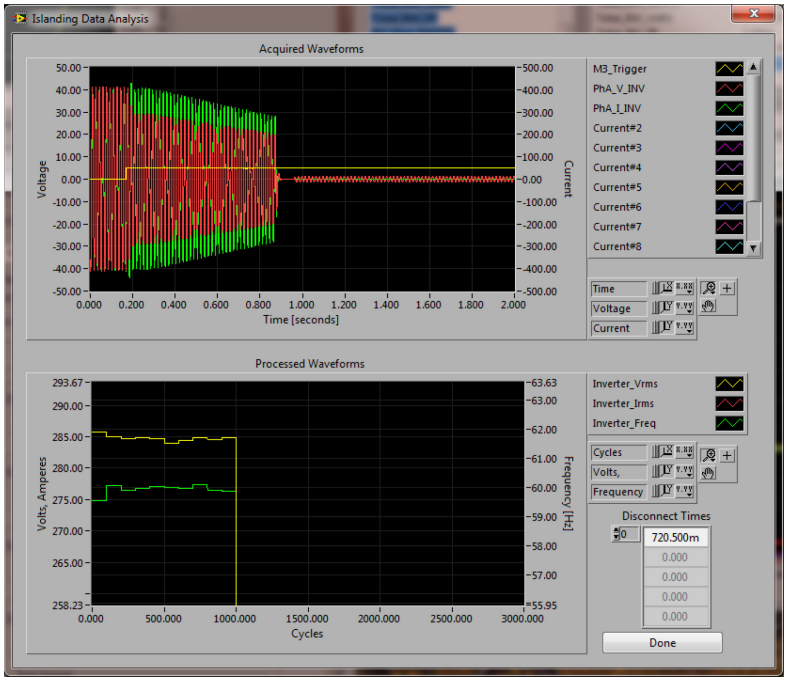
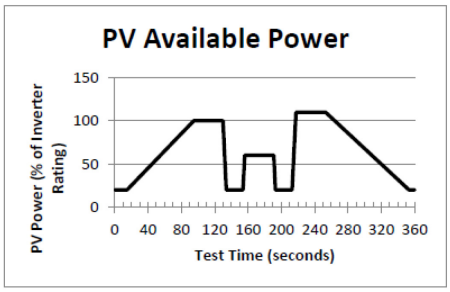


Figure 33: Screenshot showing island detection with filter (Test 3)

Technical advance 13555 was submitted, and the IP office will submit a provisional patent, but this is not yet complete at the time of this report. When complete, this will address a critical milestone.

Task 3

The Sandia test protocol [5] provides a procedure to evaluate the capabilities of the EUT under both steady state and dynamic irradiance conditions. The dynamic irradiance profile used to evaluate commanded power level accuracy is shown in Figure 1a. The profile provides a dynamic condition for the EUT to implement the commanded power level and for desired power levels > irradiance conditions allow, the EUT will only provide what is available. For dynamic conditions where irradiance supplies more dc power and the commanded generation level, the inverter must implement active controls to meet the generation level requested. Figure 34 is the test matrix that determines the power level, the ramp rate if parameter is under test, and declares the input irradiance profile to implement for each of the 6 tests listed in the matrix.



(a)

Test Number	WMax (% nameplate)	Ramp Rate (% nameplate watts/sec)	Time Delay (sec)	Timeout Period (sec)	Input PV Power Curve
Test 1	25	Default	0 (immediate)	Default (e.g., 0)	Figure A2- 1
Test 2	90	Default	300	Default (e.g., 0)	Figure A2- 1
Test 3	50	20	60	30	Figure A2- 1
Test 4	100 (default)	Default	0	Default (e.g., 0)	Figure A2- 1
Test 5	0	2	0	0 (No Timeout)	Constant at 100%
Test 6	100	2	0	0 (No Timeout)	Constant at 100%

(b)

Figure 34. Illustrating (a) Irradiance A2-1 profile and (b) Commanded power test matrix

INV2 Function Test Results

The INV2 function sets the maximum generation level as a percentage of nameplate capacity in response to a command from the simulated utility controller or a combination of local conditions, modes, schedules, etc. The function can implement a ramp rate for which the programmed generation level power must respond to and a time window within which to randomly start. A timeout period is included for reverting to the default state of the EUT. Initially, only the maximum generation level as a percentage of nameplate values will be verified and analyzed for accuracy.

The following test results show the inverter responding to communicated power level commands and the data recorded is used to determine the accuracy of the inverter to deliver the requested percentage of rated real power. Figure 35 shows the inverter responding to the power curtailment command. Table 4 shows the accuracy of the inverter's ability to deliver the commanded real power.

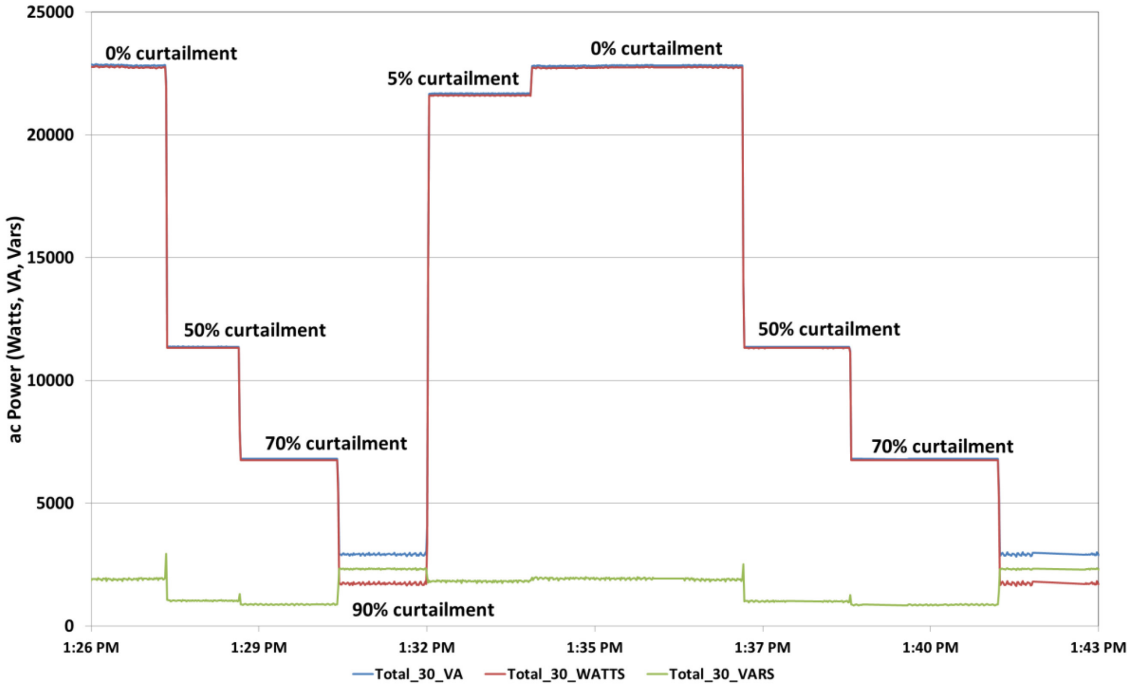


Figure 35. Commanded active power generation

Table 4. Commanded power generation accuracy, calculated vs measured

Power Curtailment	Expected power (W)	Power level (W)	% error
0%	22782	22782	0.00
50%	11391	11328	0.56
70%	6835	6759	1.11

INV3 Function Test Results

The INV3 function sets the power factor (i.e., Displacement Factor) angle in response to a command from the utility controller or a combination of local conditions, modes, schedules, etc. A ramp rate and a delay time before starting may also be included. A timeout period may be included for reverting to the default state of the EUT. Possible values for acceptable power factor ranges may be -0.5 to 0.5 or -0.8 to 0.8. It should be kept in mind that at low power levels, power factor is undefined. The manufacturer should be consulted about the expected response to a power factor command under low power output conditions. Figure 36 provides the power factor targets. The EUT produces reactive power as a percentage of real power rating and the following test results show the inverter responding to reactive power commands to the inverter. The data presented in Figure 25 displays the responsiveness of the inverter and Table 5 shows the accuracy of the inverter's ability to deliver the commanded reactive power.

For all reactive power commands over 25%, the inverter's kVA limits required it to reduce its real power output below 100%.

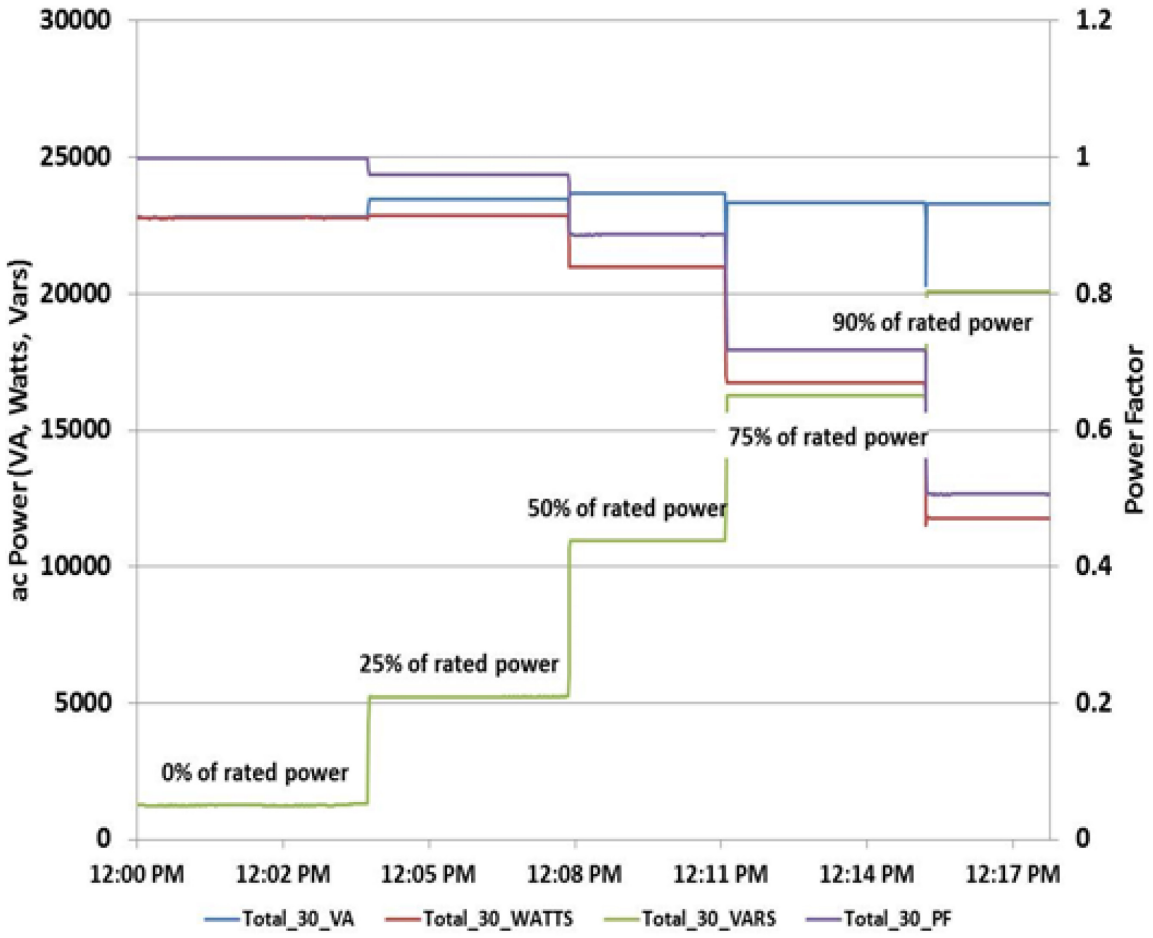


Figure 36. Commanded Power Factor Function plot shows inverter delivering commanded power factor at various power factor levels

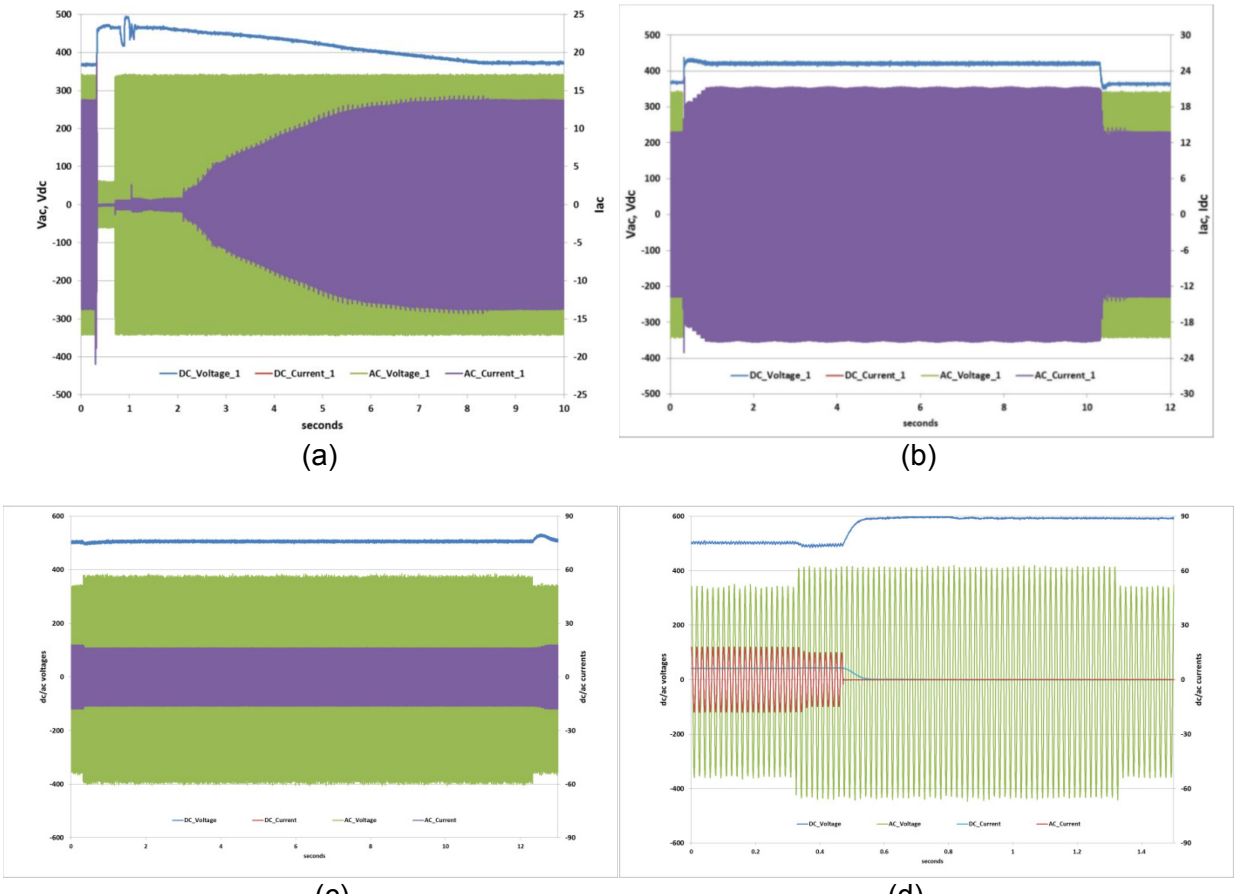
Table **5. Commanded power factor accuracy**

% of rated	Expected VAr	measured VAr	% error	PF
25	5688.6	5231.8	8.0	0.97
50	11377.6	10967.0	3.6	0.89
75	17067.2	16267.3	4.7	0.72
90	20481.7	20092.1	1.9	0.51

LVRT Function Test Results

Low voltage ride-through evaluations were conducted on an industry partner's inverter to see if it could meet the CPUC Rule 21 LVRT requirements. For these

requirements, the level of voltage sag determines the length of ride through and the mode of operation during the ride through event. If the voltage sags below 0.5 per unit (PU), the inverter must cease energizing the utility but must remain connected for duration of 1 second. If the voltage recovers above 0.5PU within 1 second, then the inverter must resume energizing the utility up to 90% of pre-event power. Figure 37 (a) shows the inverter operating at rated power and then cease energizing the simulated utility and when the voltage recovers to pre-event values, the inverter returns to pre-event current values. The plot (b) shows the inverter respond to a voltage sag that is above the 50% threshold but below the 70% threshold. The inverter must remain energizing the utility for voltage sag of this magnitude. Both plots indicate the inverter measured the voltage well within the accuracy required to make the determination of the mode in which to operate. Plots (c) and (d) show the inverter respond to an overvoltage event. In plot (c) the EUT shows it continues to energize the utility for up to 12 seconds for a surge < 120% of nominal and plot c shows a shutdown within 10 cycles for a surge that is >120% of nominal, thus adhering to Rule 21 requirements.



(a) (b)

(c) (d)

Figure 37. LVRT events are requiring different responses. (a) LV3—EUT responds with required momentary cessation for a sag < 1.5 second, (b) LV2—EUT remain energizing EPS for a sag < 11 seconds, (c) HV1—EUT remains energizing EPS for surge < 13 seconds, (d) HV2—EUT trips with required 10 cycles

L/HFRT Function Test Results

Low and high frequency ride-through evaluations were conducted on an industry partner's inverter to see if it could meet the CPUC Rule 21 LVRT requirements. For these requirements, the level of frequency sag determines the length of ride through and the mode of operation during the ride through event. If the frequency sags to LF2 region the inverter must trip within 0.167 seconds and if the frequency is in LF1 region, the inverter must ride-through for 299 seconds, see figure 38 (a). If the frequency is above (NN) region but below HF1 region, the inverter must ride-through for 299 seconds, see figure 38 (b) and for a frequency above that the inverter must trip in 0.167 seconds.

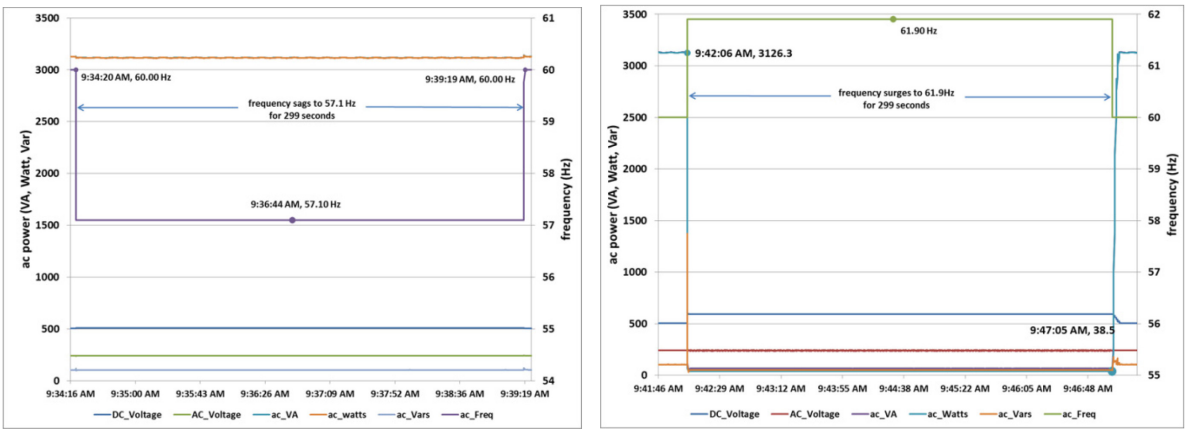


Figure 38. L/HFRT in LF1 and HF1 regions must ride through 299 seconds. (a) LF1—EUT responds with a 299 second ride-through, (b) HF1—EUT rides through for 299 seconds.

Volt-VAr Function Test Results

This evaluation validates the voltage support function – volt/VAr. The test documents the response characteristics for providing reactive power in response to a voltage anomaly. Inverters can be set to prioritize reactive or real power production with Volt-VAr functions. This priority setting defines the inverter's behavior when the inverter reaches its kVA limits. When an inverter is set to real power priority and the inverter's kVA limit is reached, reactive power limited to maintain to maximize real power production. When an inverter is set to reactive power priority and the inverter's kVA limit is reached, real power is reduced to maintain reactive power production. Figure 39 shows the inverters real power is reduced to deliver reactive power when the voltage anomaly occurs.

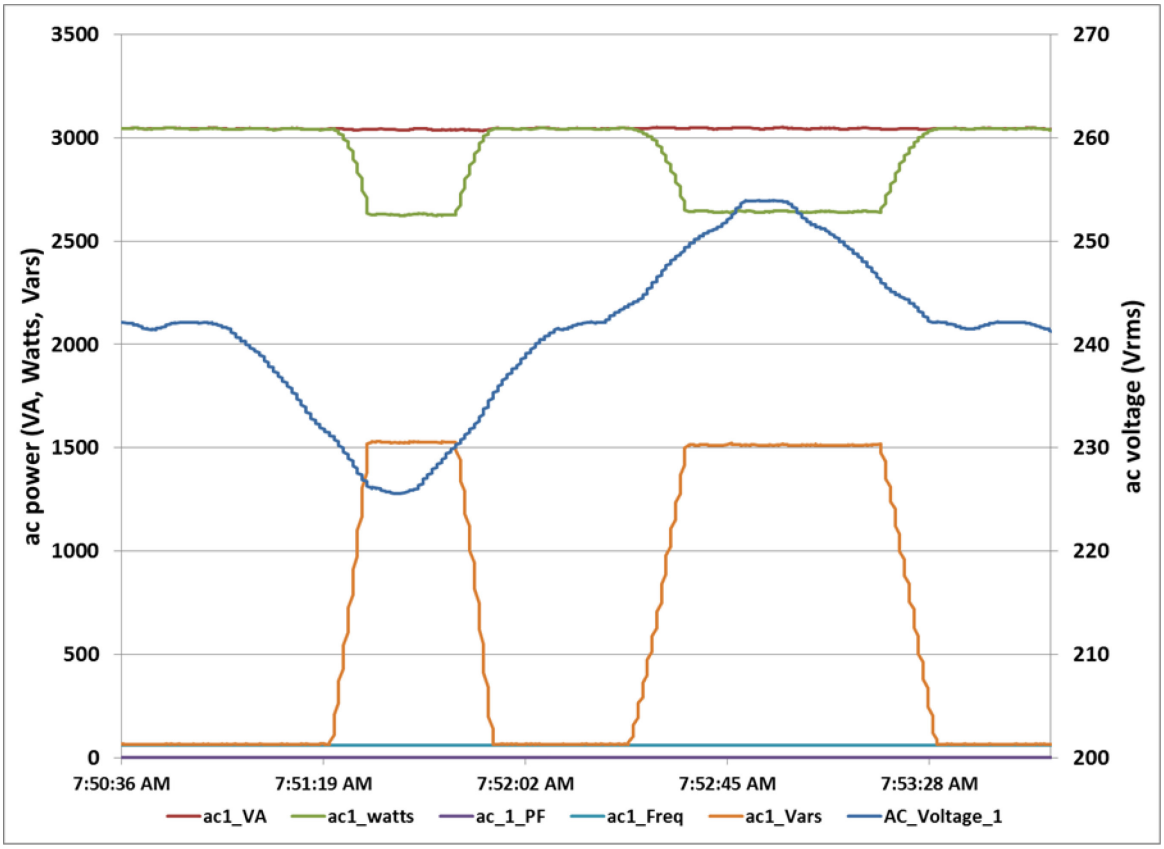


Figure 39. Volt-VAr function—Test result showing a VAr priority volt-VAr function response resulting in a reduction of real power to meet reactive power requirements

Frequency-Watt Function Test Results

With the frequency-watt curve implemented, the inverter response was analyzed during multiple frequency deviations. As shown in Figure 40, an over-frequency variation was programmed into the ac simulator and the real power generation from the inverter decreased depending on the severity of the deviation. The frequency deviations were repeated and the inverter responded accordingly. As the frequency returned to nominal, the real power generation for the inverter returned to rated power levels, indicating high precision for inverter frequency-watt functions.

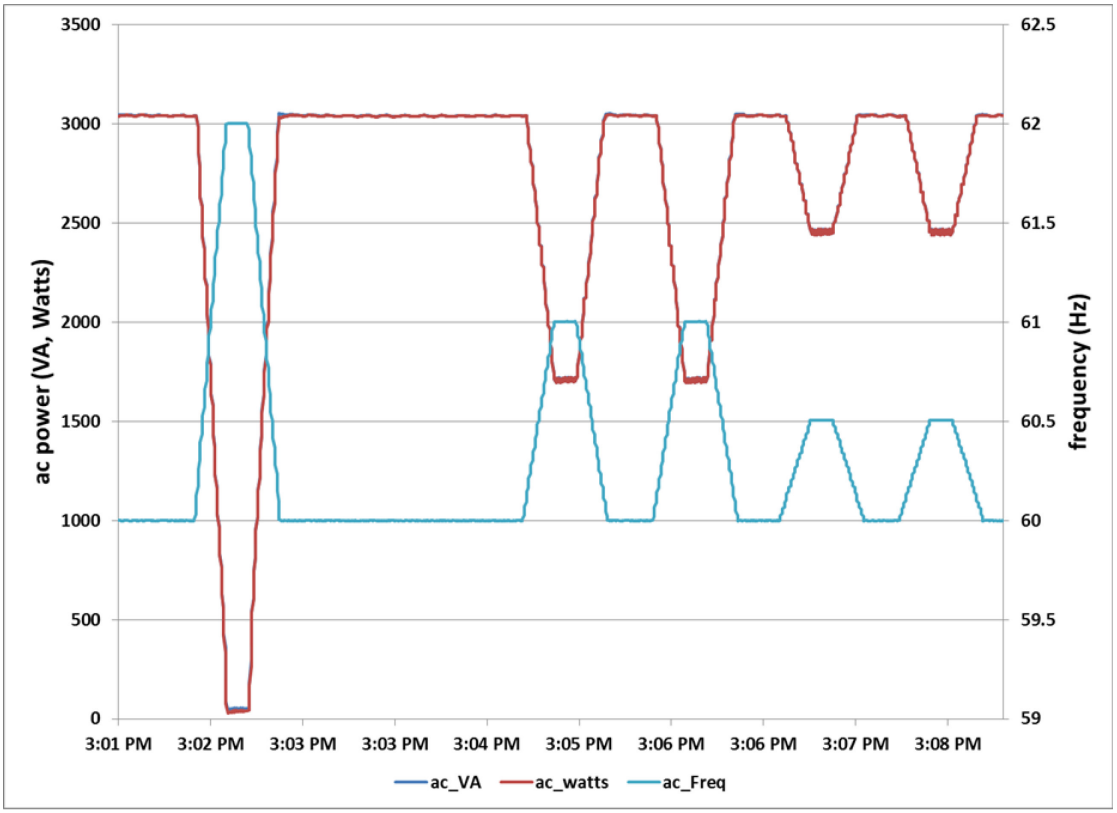


Figure 40. Frequency-Watt Function—EUT real output power is reduced as frequency increases beyond pre-programmed over-frequency power reduction value.

Anti-Islanding Evaluation Test Results

Unintentional islanding testing, with the new EPS support functions enabled, has become a process that involves quantifying the support functions and enabling these functions to the most aggressive settings, with the minimum and maximum voltage and frequency operating ranges and ride-through. Due to the number of functions that may be enabled simultaneously, the permutations are extensive, and the number of tests in UL 1741 has increased considerably. Further complicating the certification tests, if the EUT fails a particular combination of enabled functions, the suspect function will have to be modified and requantified, and the islanding test must be rerun with that particular combination of functions. Figure 41 shows the results of an extensive islanding test with the L/HVRT, L/HFRT, volt-VAr, and frequency-watt functions enabled and set to their most aggressive settings.

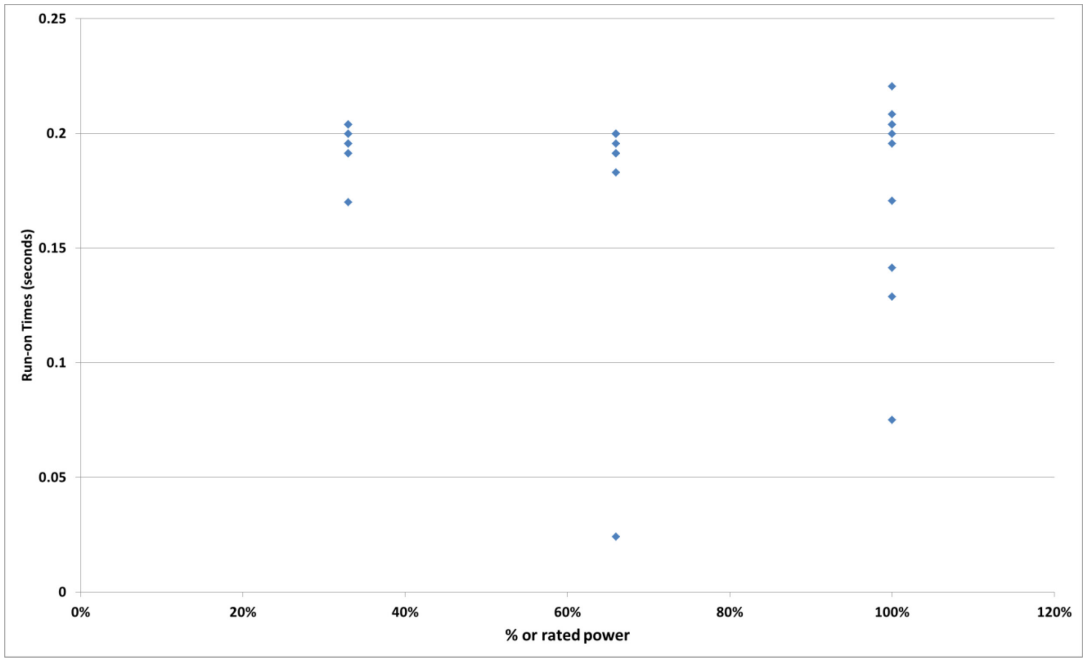


Figure 41. Anti-islanding Test Results—EUT operating with voltage and frequency ride-through capabilities enabled and voltage/frequency regulating functions enabled.

Transient OverVoltage Investigation (TrOV)

Baseline load rejection transient over voltage tests were conducted on several inverter configurations. For these tests, the inverters were operating at or close to rated current when the utility was removed, leaving minimal load remaining on the inverter terminals. Test articles included: (1) a single microinverter unit, (2) multiple (7 units) microinverter units in parallel, (3) a single single-phase residential unit, and (4) a single three-phase small commercial inverter. Results are shown in Figure 42. Therein, the worst case is a 46.4% overvoltage in Figure 42c while the others are 42.7%, 37.4% and 23.3 % for a, b and d respectively.

Furthermore, In a recent report released by NREL in collaboration with SolarCity [36], the results of a rather comprehensive LRO study were presented. Therein, test results included five commercial units, 11 power/loading scenarios, each repeated several times. The results are consistent with these tests done at Sandia (DETL) and indicate that the LRO concerns may be overstated. Therein, the worst-case result was a 200% overvoltage, but the typical values were quite a bit smaller. Thus, the concern remains, but the typical voltage amplitudes are less than anticipated.

Using Sandia generic models, some of these LRO tests were repeated indicating similar results. An example is shown in Figure 43. The simulation starts with the inverter operating with Volt-VAr and Frequency-Watt functions enabled, supplying rated power of 49.4kW. Of that power, 80% was being consumed by a local load, and 20% was being delivered to the grid. At time t = 12 seconds, the grid was disconnected. Figure 43 shows the phase voltage transients. Phase B has the highest peak voltage, at 483.9V.

Additional work is ongoing to investigate Ground Fault Overvoltage in simulation.

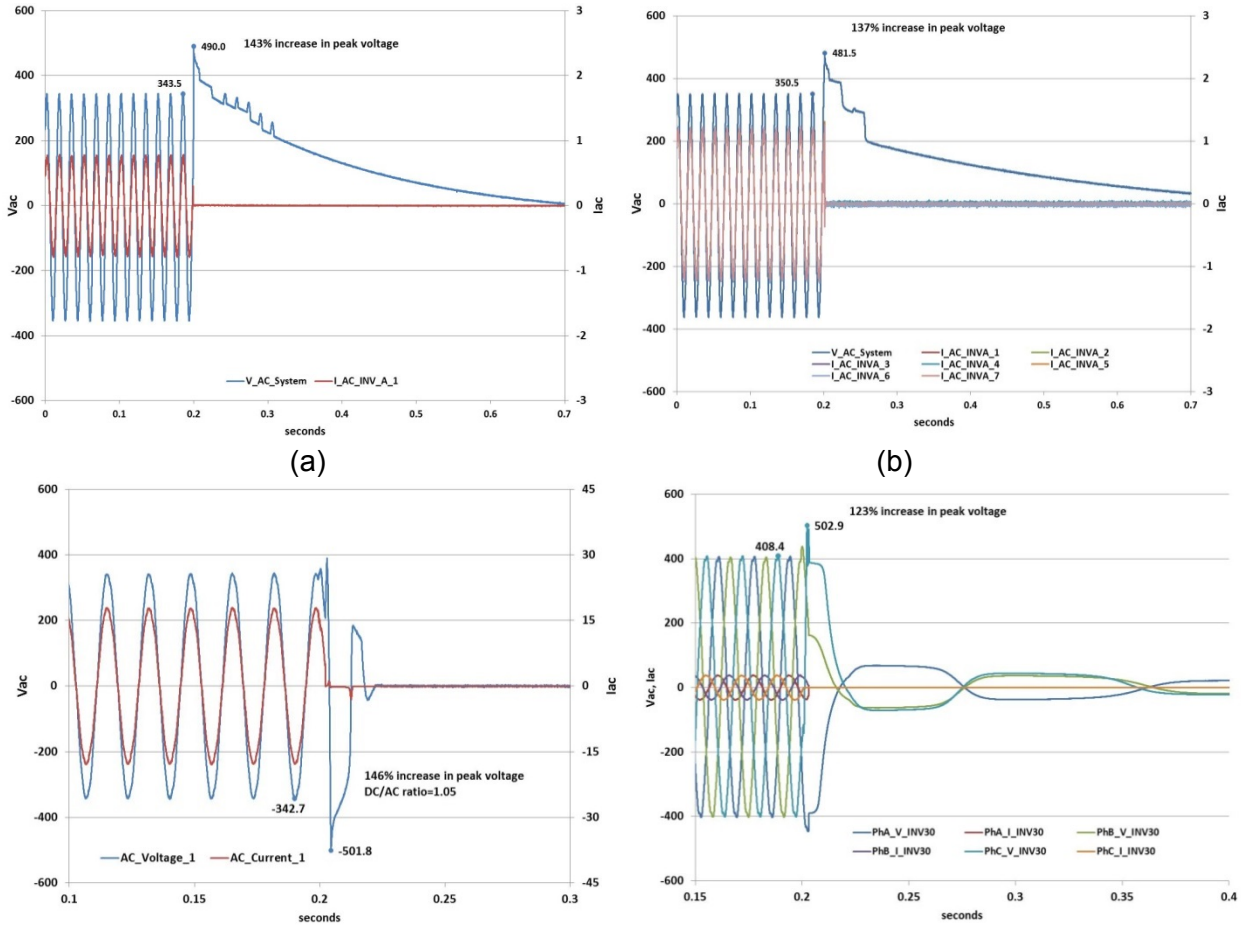


Figure 42: (a) waveform of a single microinverter, (b) waveform of 7 microinverters in parallel, (c) waveform of a 1-Ph inverter, (d) waveform of a 3-Ph inverter

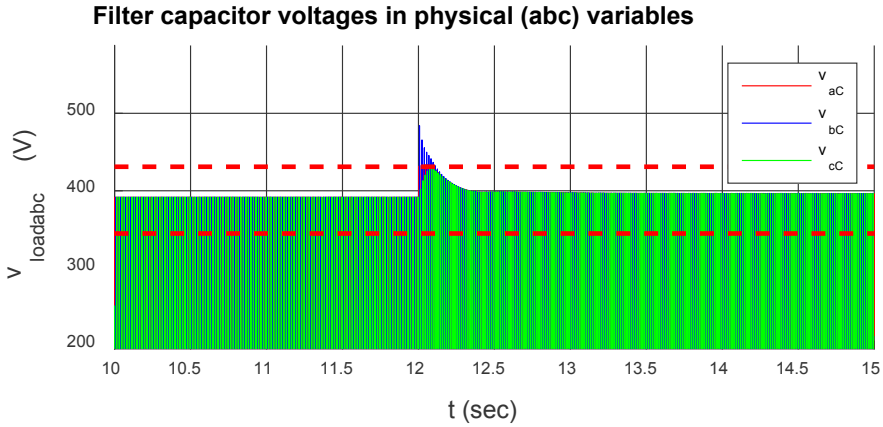


Figure 43: Output voltage transient on 3-phase inverter in simulated LRO test with voltage/frequency regulating functions enabled

Cyber Security

In general, the development of a codified cyber security test protocol will be very difficult to define. Instead a red-teaming methodology may be more appropriate. As part of this effort, Sandia's IDART assessment methodology was applied to a commercial inverter that has remote control capabilities. This included the development of an attack graph and an assessment of cyber vulnerabilities. The results are documented in an OUO-Category 3 report [36] in development.

Significant Accomplishments and Conclusions:

In this project, several advancements have been made to further the adoption of advanced inverter functions. This research has clarified the impact of these functions on anti-islanding and developed new alternative islanding detection schemes. This project has also developed new testing protocols, applied these successfully to manufacturer hardware, and helped support their adoption in the broader community.

Anti-Islanding

Through experimentation and the development of several manufacturer-specific transient-level inverter models, this project helped to clarify the impact of multi-inverter configurations and GSFs and V/FRT on the efficacy of anti-islanding. These models were developed by NPPT in collaboration with manufacturers and with the use of data collected at Sandia's DETL lab. This allowed for islanding performance to be quantified in terms of run-on times (ROTs) for a large number of scenarios.

In general, the effect of GSFs and V/FRT on anti-islanding appears to be somewhat overstated. Anti-islanding efficacy is degraded somewhat by these functions since they tend to cause an increase in ROTs in simulation when the functions are enabled; however, ROTs never reached noncompliance (ROT>2 sec). One experiment, however, resulted in ROT>2sec when inverters from different manufacturers that had GSF and V/FRT enabled and were connected together on one bus. The community thus remains concerned about islanding.

To address the potential for poor anti-islanding performance in high penetration PV systems, two new anti-islanding methods were developed. The first is based on powerline carrier and its efficacy is not mitigated by GSFs or V/FRT since it allows a more direct way of determining grid connection regardless of inverter dynamics. This method relies on voltage injection instead of current injection and may be implemented by utilities more economically. It seems likely a form of this technology will be implemented in the future with high PV-penetration systems. A provisional patent was submitted for this method. The second method involves adjusting the autonomous anti-islanding controls to "work with" the GSFs and V/FRT. This method shows promise in simulation, but our attempts to get experimental validation were disappointing. The test indicated the collaborative controls may have worked, but the test needs to be repeated, and the industry partner encountered financial problems before this could happen. A provisional patent for this approach is in development. It is believed this approach would likely be implemented in the short term and eventually replaced by powerline carrier implementations in the long term.

Test Protocol Development and Validation

Through this effort, Sandia lead the way in developing a test procedure to validate the IEC61850-90-7 object models that describe the advanced inverter EPS support functions. Specifically, Sandia worked with manufacturers and industry partners to identify success metrics for adherence to IEC61850-90-7, developed the test procedure and exercised the procedure on manufacturer hardware. This process demonstrated IEC61850-90-7 compliance in four early adopters of EPS functions and *testability* of the

protocol. Sandia also participated in IEEE-lead forums and working groups to socialize the process and progress. This Sandia-lead effort created momentum in the development and adoption of these functions.

In addition to EPS function performance, this test protocol development effort included investigations of Transient Over-Voltage (TrOV) and Cyber security topics. These were brief efforts. For TrOV, Sandia and NREL did some investigations in parallel that both indicated that load rejection overvoltage (LROV) is underwhelming as a problem. Ground-Fault Overvoltage (GFOV) has not yet been properly characterized. The Sandia consensus is that a Cyber security test protocol is not practical in the sense of establishing compliance for a set number of criteria. Instead, Sandia experts recommend a Red Team process such as the *Information Design Assurance Red Team* (IDART). However, the testability of this process has not been established in the context of grid-tied inverters. However, in a DETL-run experiment with a single diesel generator, a resistive load, and a PV inverter with frequency-watt function, a scenario was demonstrated wherein adjustment of a single parameter, that is settable through communications, could cause instability in a small power system.

Inventions, Patents, Publications, and Other Results:

The progress and findings of this project have resulted in one provisional patent and have been documented in four conference papers, six SAND reports and two public presentations.

Provisional Patents:

"Subharmonic Power Line Carrier Based Island Detection Systems and Methods." US Provisional Patent Application No. 62/193,373, filed July 16, 2015.

Conference Papers:

Gonzalez, S.; Johnson, J.; Neely, J.; "Electrical Power System Support-Function Capabilities of Residential and Small Commercial Inverters"; Photovoltaics Specialists Conference (PVSC2015); New Orleans, LA; June 14-19, 2015.

Ropp, M.; Perlenfein, S.; Schultz, D.; Mouw, C.; Gonzalez, S.; Neely, J.; Mills-Price, M.; "Practical Considerations in Application of Correlation-Based Islanding Detection with SynchroPhasors"; Photovoltaics Specialists Conference (PVSC2015); New Orleans, LA; June 14-19, 2015.

Perlenfein, S.; Ropp, M.; Neely, J.; Gonzalez, S.; Rashkin, L.; "Subharmonic Powerline Carrier (PLC) Based Island Detection," Applied Power Electronics Conference and Exposition, 2015. APEC 2015. Thirtieth Annual IEEE, 15-19 March 2015.

Gonzalez, S.; Neely, J.; Ropp, M.; "Effect of Non-unity Power Factor Operation in Photovoltaic Inverters Employing Grid Support Functions"; IEEE Photovoltaics Specialists Conference (PVSC 2014); Denver, Colorado; 8-13, June 2014.

Technical SAND Reports:

J. Neely, S. Gonzalez, M. Ropp, D. Schutz; "Accelerating Development of Advanced Inverters: Evaluation of Anti-Islanding Schemes with Grid Support Functions and Preliminary Laboratory Demonstration"; Sandia National Laboratories Technical Report; Albuquerque, NM; SAND2013-10231; November 2013.

J. Johnson, S. Gonzalez, M. Ralph, A. Ellis, R. Broderick; "Test Protocols for Advanced Inverter Interoperability Functions—Main Document"; Sandia National Laboratories Technical Report; Albuquerque, NM; SAND2013-9880

J. Johnson, S. Gonzalez, M. Ralph, A. Ellis, R. Broderick; "Test Protocols for Advanced Inverter Interoperability Functions—Appendices"; Sandia National Laboratories Technical Report; Albuquerque, NM; SAND2013-9875J.

Neely, S. Gonzalez, M. Ropp, S. Perlenfein, D. Schutz, L. Rashkin; "Advanced Inverters: Evaluation of Multi-Inverter Anti-Islanding with Grid Support and Ride-Through and Investigation of Island Detection Alternatives"; Sandia National Laboratories Technical Report; Albuquerque, NM; SAND2016-xxxxx; January 2016 **(In preparation).**

J. Daley, P. Schulz, L. A. Dawson, J. Neely; "Accelerating Development of Advanced Inverters: Evaluation of Cyber Security Vulnerabilities"; Sandia National Laboratories Technical Report; Albuquerque, NM; SAND2016-xxxxx; January 2016 **(In preparation).**

S. Gonzalez, J. Neely, J. Delhotal; "Advanced Inverters: Evaluations of Advanced Inverter Grid Support Functions"; Sandia National Laboratories Technical Report; Albuquerque, NM; SAND2016-xxxxx; January 2016 **(In preparation)**

Public Talks:

Neely, J.; Ellis, A.; Gonzalez, S.; Johnson, J.; "Integration of Advanced Inverters for Increased PV Penetration" ; Alternative Energy Industry Session Presentation; Applied Power Electronics Conference (APEC 2015); Charlotte, NC; March 18, 2015.

Neely, J.; "Integrating Renewable Energy: Preparing the Grid for an 'All of the Above' Energy Strategy"; Sigma Xi Young Investigator Award Lecture; University of New Mexico; November 14th, 2013.

Path Forward:

Considerable R&D work is still needed to enable the adoption and full potential that advanced inverter functions have to offer. Firstly, the effect of these functions on the greater grid needs to be better understood. Thus, path forward efforts should include grid-scale simulations that include volt-VAr, frequency-watt and V/FRT to be included in PV plant models and simulated using a tool such as GE's PSLF dynamic simulation platform. Secondly, work should continue on the development of the powerline carrier and collaborative controls autonomous anti-islanding methods. This will require a manufacturer or utility to sponsor further development. Finally, identification of a single standardized autonomous anti-islanding scheme industry can agree on would be of great value; these may be collaborative controls or some aggregation of methods like what is used in Germany and Japan

Test protocol refinements will continue, which includes revisions to IEEE 1547.1 and UL 1741SA. In addition, Sandia needs to continue its role in testing and troubleshooting EPS function implementation for manufacturers. Sandia has identified various performance and possible hardware challenges when conducting evaluations on industry partners' inverters. With the limited assessments conducted, all samples have non-compliance issues and manufacturers have expressed a strong desire to address these issues.

There has been a great deal of concern recently over transient overvoltage. Recent tests by NREL and Sandia have indicated that the effect of load rejection overvoltage is underwhelming. However, additional studies should be done to better characterize ground fault overvoltage. This particular concern may be investigated in simulation but is difficult to test properly in hardware.

Finally, additional R&D effort is needed to better define the cyber security assessment process. More mature methods such as Sandia-developed IDART are effective but may pose problems with "testability" due to the resources needed for the assessment.

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